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DEVELOPMENT OF PILOT PRODUCTION CAPABILITIES FOR SILICON CARBIDE POWER DEVICES AND INTEGRATED CIRCUITS

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The effort funded by this contract encompassed two principal objectives: First, the creation of a silicon carbide device prototyping capability at Mississippi State University by the creation of the first SiC fab line independent of commercial control. Secondly, the demonstration of a power Schottky barrier diode (SBD) prototyped in preproduction lot size. This final report documents the detailed description of the design, fabrication methodology, and testing results of the 15,000 SBD's fabricated and tested. The principle accomplishments of the funded effort are: The completion of a SiC foundry including fabrication services. Schottky barrier diodes were fabricated with reverse blocking characteristics averaging 500 volts, and with on-state forward voltage drops of <2.5 volts at 100 amps/cm2. Finally, a commercial supplier of advanced and specialty discrete power devices evaluated and subsequently used the SBD's developed under this program to announce and release the first-ever commercial SiC power device using their proprietary high-power-density packaging, thus fulfilling the initial promise of the prototype manufacturing facility.

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EXECUTIVE SUMMARY

Contract F33615-00-C-2010 was awarded on 29 February 2000 and modified twice to a total value of $3,199,698. The contract expired on 31 December 2001 and this document represents the final deliverable.

The effort funded by this contract encompassed two principal objectives:

1. The creation of a silicon carbide semiconductor device prototyping capability at Mississippi State University by the creation of perhaps the first SiC fab line independent of commercial control: the Mississippi Center for Advanced Semiconductor Prototyping (MCASP).
2. The early demonstration of a power Schottky barrier diode (SBD) prototyped in pre-production lot size (i.e., many more parts than is typical of research).

As the contract was awarded in two principal increments, these two objectives were funded sequentially. Both technical challenges were fully met by the conclusion of the contract. Since the latter effort involved the principal technical deliverables of the contract, the following document focuses mainly on a detailed description of the design, fabrication methodology, and testing results of the approximately 15,000 SBD fabricated and tested in this program. However, the activity of creating MCASP was by no means a secondary effort and it required the dedicated effort of a large team of engineers and students at Mississippi State University. The principal investigators of this project wish to

acknowledge Mr. G. Evan Burnett for the report that follows, which was largely authored by him in partial fulfillment of the degree requirements for his Master of Science in Electrical Engineering at Mississippi State University.

The principal accomplishments of the effort funded by this contract can be summarized as follows:

- The completion of a SiC foundry (MCASP) in a temporary location on the campus of MSU, including fabrication services ranging from SiC epitaxial growth to 0.8 μm photolithography to multiple types of oxidation, to deposition of multiple contact metals, through automated wafer-scale testing of high-voltage (typically ranging 600 to 1200 V, but capable of up to 5 kV) power devices. Appendix C summarizes this capability.
- The completion of SBD lot 02D in which nearly 20 wafers were processed yielding over 15,000 individual parts. After packaging, reverse bias breakdown voltages over 500V at 0.1 A/cm^2 and an on-state forward voltage drop of less than 2.5V at 100 A/cm^2 were demonstrated. A 0.65-0.85 eV barrier height was extracted from the SBD's using I-V measurements. Field plate terminated devices demonstrated consistent, low standard deviation breakdown voltages and low leakage currents. The argon implanted devices demonstrated a higher breakdown voltage with higher leakage currents and a higher standard deviation. It was proven that the diodes followed the thermionic field emission model for up to one third of the breakdown voltage.
- The involvement of a major supplier of advanced and specialty discrete semiconductor devices to the prime contractors supplying the Department of Defense

in packaging and evaluating the commercialization potential of SiC SBD's. This company, Microsemi Inc., subsequently announced the commercial availability of SBD's in the state-of-the-art high-power-density Powermite® package, thus fulfilling the initial promise of the MCASP concept funded under this contract.

The MCASP concept is continuing under a different four-year contract vehicle with the Air Force Research Laboratory to leverage this early success with the development of a high-performance SiC switch based on the vertical junction field effect transistor. In the spirit of the effort documented here, every effort will be made to introduce this device technology through the normal supplier chain so as to fulfill the promised benefits of SiC semiconductors into relevant DoD weapon systems.

CHAPTER I

INTRODUCTION TO THE SiC SCHOTTKY BARRIER DIODE

The Mississippi Center for Advanced Semiconductor Prototyping (MCASP) at Mississippi State University is currently developing a line of Silicon Carbide Schottky barrier diodes (SBD). SBD's are unipolar devices that are mostly used in demanding switching applications that require low reverse recovery transients [1]. Unlike the bipolar p-n junction diode, the SBD has a negligible reverse recovery time because of a lack of minority carrier injection. Another advantage of SBD's is that they are relatively easy to fabricate compared to other rectifiers [2]. With the use of SiC as the SBD semiconductor material, it then becomes a high-temperature, high-power device in addition to a high-frequency device. SiC has been researched and developed over the past 40 years as a wide bandgap, high thermal conductivity semiconductor material with robust mechanical properties [3]. By using SiC, devices 20 times smaller than correspondingly rated Si devices can be realized [4]. The SiC SBD is currently being developed for use in several different applications, all requiring high current, high voltage, and high temperature device switching behavior for such applications as motor-drives, high efficiency converters/inverters, medical defibulators, and space applications. However, to perfect the performance of SiC SBD's many improvements must be made in the areas of design,

fabrication and materials used, in order to obtain both high reverse breakdown voltage and high forward bias currents with a high level of device yield.

Previous Investigations

In the development of SiC Schottky barrier rectifiers, there have been several investigations that have produced some notable results. Circular SBD's ranging in size from 100 to 130 μm in diameter have been fabricated using 4H-SiC at Kyoto University [5]. These rectifiers have breakdown voltages on the order of 1000V with 100A-cm^{-2} forward current density capabilities. The Kyoto SBD's were fabricated with a Ti Schottky contact, Ni ohmic backside contact, and the surface was terminated with a B^+ implant to reduce surface electric field stress. The doping density (n-type) used was ~3 x 10^{15} cm^{-3} – 2 x 10^{16} cm^{-3} with an epilayer thickness of 10 μm. It was found that the Ti Schottky contact minimized power loss by controlling the barrier height with its metal work function, which lowered the reverse leakage current and lowered the forward voltage drop of the rectifiers [5].

A group of French researchers have concentrated on the forward bias characteristics and effects of growth pits on 4H-SiC, 10 A-cm^{-2}, 400μm diameter circular devices [6]. They used an n-type epilayer of 1 x 10^{16} cm^{-3} with a 10 μm thick epilayer. It was reported that the breakdown voltage was greater than 1000V if the forward bias voltage was ~1V with ideal characteristics. This shows an important linkage between forward and reverse characteristics in SBD's. They created a model of what was observed based on a dual on-state that was related to the defects in the materials. The

defects in their rectifiers suggested two corresponding different ideality factors for forward bias and two different barrier heights [6].

The Power Semiconductor Research Center (PSRC) at North Carolina State University has reports of 4H-SiC, Al doped p-type, 600V SBD's that are 230 μm in diameter [7]. These devices have a very high forward drop of 6V-13V with a current density of 100 A-cm^{-2}. The high forward bias voltage drop may be due to their method of dual metalization. Their method consists of depositing 1000 Å of Ti followed by 1000 Å of Al. These measurements were performed on only 40 working diodes of 4H-SiC [7].

A few years earlier, the PSRC reported 330 μm 4H-SiC n-type rectifiers with a reverse breakdown averaging 820 V and forward bias voltage drop of less than 1.1 V at 100 A-cm$^{-2.}$ These were 1 x 10^{16} cm^{-3}, 10 μm thick nitrogen doped devices that again had a dual Ti/Al Schottky contact as well as a blanket Ti/Al layer for a backside ohmic contact [8].

Fuji Electric Corporate Research and Development has reported 200 μm, Ti/Al Schottky contact, Ni ohmic contact SBD's with a p-type guard ring termination [9]. The guard ring was fabricated using their technique for creating pn junction diodes by using a mesa-style device. A comparison was made between their conventional method of fabricating the SBD's with and without the terminating ring. This report shows a direct improvement of 200-400V in reverse breakdown voltage with the termination structure. Reverse bias voltages up to 600V were reached by these devices [9].

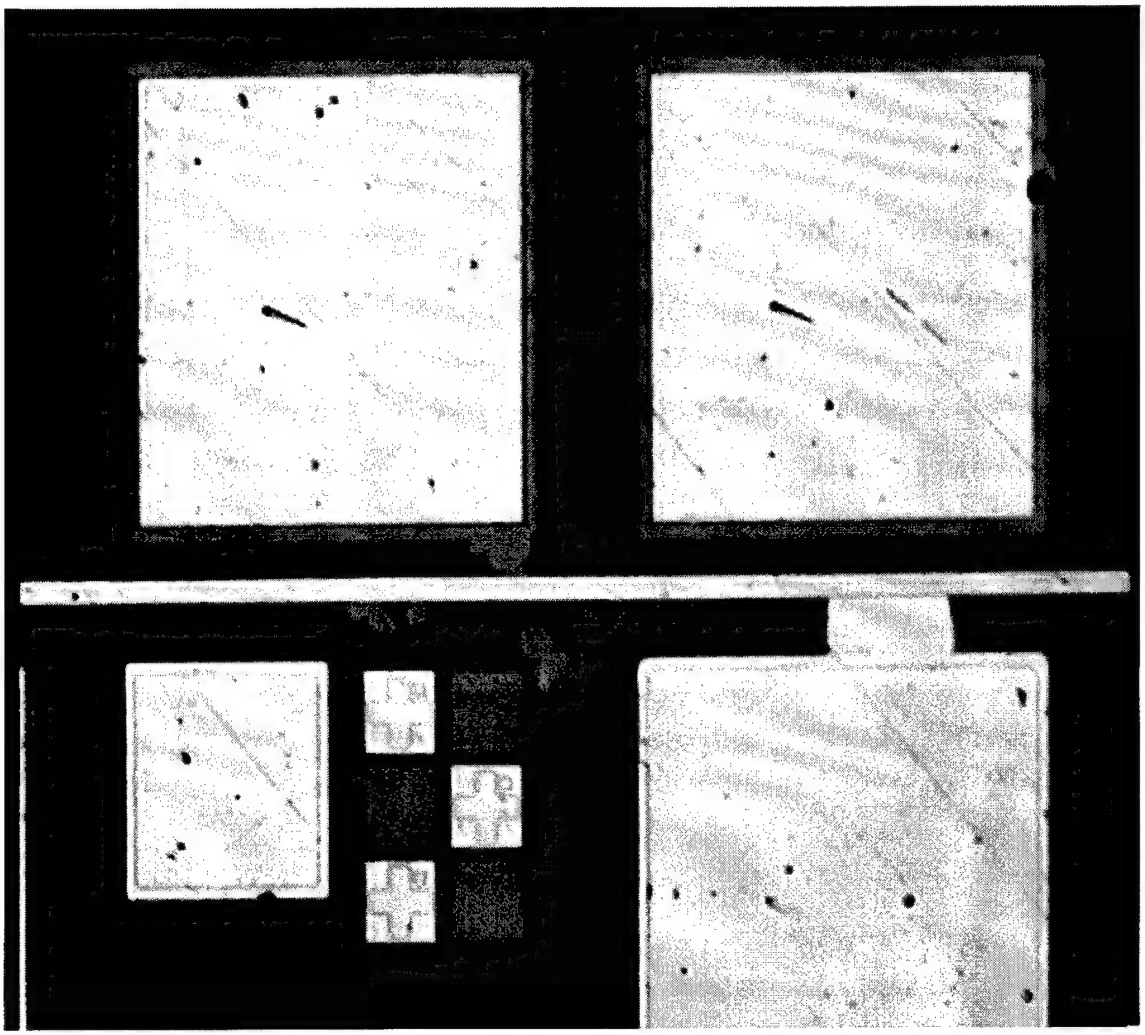

Figure 1.1: SiC SBD's fabricated at MCASP

1kV, 4H-SiC SBD's have been demonstrated by the University of Cincinnati [10]. These field plate overlap devices have a circular geometry with a diameter ranging from 30-240 μm. These devices were fabricated using a 10 μm thick epilayer with an n-type doping density of $10^{15} - 10^{16}$ cm^{-3}. Ni ohmic contacts along with Ni or Pt Schottky contacts were used for fabrication. The purpose for the two different Schottky metals was to compare the different barrier heights which are known to be strongly dependent on the metal work function. A "good yield" was reported on the diodes, but not quantified [10].

Baliga *et al.* investigated 300 μm, circular, titanium SBD's with an argon implant edge termination [11]. They investigated the effects of the dose of the implant compared to breakdown voltage. The diodes were fabricated by depositing an n-type, 10μm epilayer with a doping density of 8×10^{15} cm^{-3} on a 4H-SiC substrate. These rectifiers reached voltages up to 1333V with currents just under 1mA. Forward bias specifications were not discussed [11]. Two years earlier, Baliga along with the PSRC performed similar investigations using a slightly higher doping density of 2.1×10^{16} cm^{-3} on 6H-SiC [12]. The same sized circular devices were fabricated using titanium and aluminum for the Schottky contacts. Again they used various doses of argon implant for their terminations. The diodes had reverse breakdown voltages up to 1020V. Again, nothing was reported for forward bias, but a correlation was supported further: a higher dose resulted in higher breakdown voltages, but also resulted in higher leakage currents [12].

Field plate overlap terminated devices were fabricated at the University of South Carolina [13]. This group investigated the improvements made in their SBD's by fabricating 150 μm devices without termination and 150 μm devices with a 50 μm

overlap (i.e. field plate) on each side. The rectifiers were fabricated on a p-type epilayer that was 10 μm thick with a doping density of 6 x 10^{15} cm^{-3}. The terminated devices displayed forward bias current densities 2-3 times better than the unterminated devices, and displayed a reverse bias breakdown voltage ~2 times higher. Forward current densities were reported at 50 A/cm^2 at a voltage of –5V. Reverse bias breakdown was reported as being greater than 1000V with very low leakage [13].

Results from the previous investigations cited are tabulated in table 1.1.

Yield Considerations

Several issues should be considered when design engineers try to improve the yield of devices produced from a single wafer. Two main topics directly affecting parametric yield are device termination and device area scaling. Device termination is important for decreasing the chances of breakdown caused by electric field crowding, but in most cases, it produces a side effect of increased leakage currents. Also, increasing the contact area improves forward bias current density capabilities, but this has a negative effect of increasing the chance of material defects residing within the device structure. This creates a design dilemma that complicates the design and manufacturing of the SiC SBD. As mentioned earlier in the literature review section, several groups have performed comparisons between different device sizes as related to breakdown voltage characteristics. Many others compared different types of terminations as related to breakdown voltage. Purdue University and Cree, Inc. have specifically investigated the effects of area scaling and the most effective means of terminating devices.

Table 1.1

Literature Review Results

	D [μm]	V_R [V]	J_R [A/cm²]	V_F [V]	J_F [A/cm²]	Anode	Polarity	Polytype	Termination	Reference
Kyoto University	130	1000	10	1.67	100	Ti	n-type	4H	B+implant	[5]
Thompson-CSF	400	1000	N/A	1	100	Ti	n-type	4H	None	[6]
PSRC	230	600	10	6	100	Ti	p-type	4H & 6H	none	[7]
PSRC	330	820	10	1.1	100	Ti/Al	n-type	4H	none	[8]
Fuji	200	600	1	N/A	N/A	Ti/Al	n-type	6H	Guard ring	[9]
Baliga et al	300	1333	N/A	N/A	N/A	Ti	n-type	4H	Ar implant	[11]
Baliga and PSRC	300	1020	1	N/A	N/A	Ti/Al	n-type	6H	Ar implant	[12]
University of South Carolina	250	1000	1	-5	50	Al	p-type	6H	Field plate	[13]
University of Cincinnati	240	1000	N/A	1.78	100	Ni & Pt	n-type	4H & 6H	Field plate	[10]
Purdue	1200	1720	0.1	2	100	Ni & Ti	n-type	4H	B+implant	[14]
Cree	150	800	0.1	1.88	100	Pt	n-type	4H	various	[15]

Purdue has related reverse leakage currents to area scaling with their 100 μm – 1200 μm boron implanted devices, which display 1720V of reverse breakdowns [14]. Their Ti and Ni Schottky rectifiers were fabricated using 13μm of 3.5 x 10^{15} cm^{-3} nitrogen doped (n-type) epilayers. Purdue performed additional studies in order to relate contact size to breakdown voltage for the purpose of finding the optimal circular contact size. They also performed a comparison between argon and boron implant regions using both a blanket-style implant and a guard ring implant. They reported that an increase in contact size yielded a decrease in breakdown voltage. It was also noted that their argon edge terminated devices produced a much larger leakage current than their boron implanted devices [14]. Clearly, the choice of edge termination technology is important to subsequent device performance.

Cree has performed extensive investigations for various types of terminations on SBD's including guard ring terminations, field plate terminations, double implanted field rings, and single and double trench rings [15]. To perform these comparisons, they fabricated four complete wafers of 54 diodes each. The wafer structure consisted of equally distributed 50, 100, and 150 μm diameter diodes using three diodes with no termination, six diodes with the guard ring, nine with the field plate, nine more with a single implanted field ring, nine with double implanted field rings, nine with a single trench implanted ring, and finally nine with double trench implants. Each diode was fabricated using an n-type epilayer of 0.8 - 1.5 x 10^{15} cm^{-3} doping density with a 13μm thickness. Each wafer of these fabricated devices produced in their study had a minimum yield of 22% and maximum yield of 67% with the single field ring. These devices

produced 500-800V breakdowns, which again directly scaled according to the type of termination used in addition to the size of the rectifier [15].

Area scaling is mostly affected by defects in materials and fabrication techniques. Neudeck has performed many studies on the defects of SiC alone and in fabricated devices [16]. In one of his investigations, he fabricated $1mm^2$ pn diodes on a 4H-SiC substrate to observe the effects of micropipe defects in these devices. Micropipes are holes or "pipes", typically 1-10μm in diameter that can extend over large distances within the substrate crystal [17]. He reported that 80% of the devices failed below 500V due to the micropipe defects. This was well below the calculated and simulated value, which assumed no micropipe defects. The estimated density of micropipes, as specified by the substrate vendor, was on the order of 100 cm^{-2} in this experiment. Two main mechanisms in the formation of micropipes were suggested. The first says that micropipes are hollow core screw dislocations that propagate along the c-axis from the seed crystal during the substrate growth process [16]. The second formation mechanism suggests that contaminant particles could be introduced in the substrate growth process. Regardless of the origin, the micropipes are a major performance limiting defect in large area SiC SBD's [16]. Unfortunately, these defects propagate into the epitaxial layer from the substrate.

Neudeck performed a similar experiment with smaller rectangular pn diodes less than 5×10^{-4} cm^2 [18]. This work resulted in the observation of another defect known as the elementary screw dislocation. These defects are similar to micropipes, except that they are not hollow and are of a smaller diameter. Elementary 1C screw dislocations (the "1" denotes a Burger's vector of 1 unit and the c denotes the dislocation is along the c-

axis) are about 100 times more common in SiC substrates than are micropipes. A typical concentration of 1C screw dislocations is on the order of 1 x 10^4 cm^{-2}. Again, these defects originate either during the substrate growth process or from the seed crystal. The end effects are the same: devices on material with a higher concentration of screw dislocations have a higher failure rate. The devices without these dislocations do not prematurely fail [18].

A final source of defects which affect yield is the device fabrication process. The actual fabrication of the SBD can cause damage to the device. The best example of this is the formation of growth pits during the epitaxial growth process. These are caused by particulates on the substrate during growth and/or polytype control problems. A common failure resulting from growth pits is the presence of a microplasma during device operation, which eventually becomes catastrophic failure points in the device. In addition, polishing and other material preparation can cause severe damage to the surface of the device, but significant advances have been made toward eliminating such manufacturing process yield problems [19].

Thesis Scope and Organization

The Mississippi Center for Advanced Semiconductor Prototyping (MCASP) has designed and fabricated diodes expected to perform in high power applications. Device characterization and statistical yield information is needed on these high voltage, high current devices to provide MCASP with an insight into further development of their Schottky rectifiers. The devices were fabricated using 10 μm thick n-type epilayers with an intended doping density of 5 x 10^{15} cm^{-3}. Ti Schottky contacts were patterned using a metal lift-off process. Ni ohmic contacts with Argon implant terminations on one half of

the wafer and field plate terminations on the other half were used for 1mm^2 devices. The goals of these devices were to accommodate a reverse bias breakdown of 600-800V at a leakage of less than 50uA. In addition, a forward bias current of 1A with a voltage drop of less than 2.5V is required. This thesis will report on the complete details of a yield investigation on these devices along with a comparison of the two terminations employed. Full device characterization of this specific lot of fabricated diodes is reported. This thesis will also provide deductions of device defects related to material defects and offer insight to improvements that can be made in the production of SBD's by investigating problems associated with sub-standard devices such as area scaling, termination problems with the field plate and Ar implant, and other possible fabrication issues. Such investigations have not been previously performed on square Schottky diodes, and only Purdue has reported a circular device with a larger contact area than will be described here.

This work is divided into four main sections. First, in Chapter Two, a discussion of the theory behind SBD's will be provided to assist in understanding related device characterization issues. This chapter will begin with the basic theory of operation of the SBD, followed by practical design considerations, and will conclude with SBD fabrication techniques. Chapter Three will discuss the experimental setup and will be broken down into the equipment used in the wafer-level testing of the devices and then into the two different types of testing performed. The next chapter will present the results of testing performed on the SBD's. Chapter Five will discuss and analyze the test results in detail. Finally, Chapter Six will summarize the conclusions and accomplishments of this work.

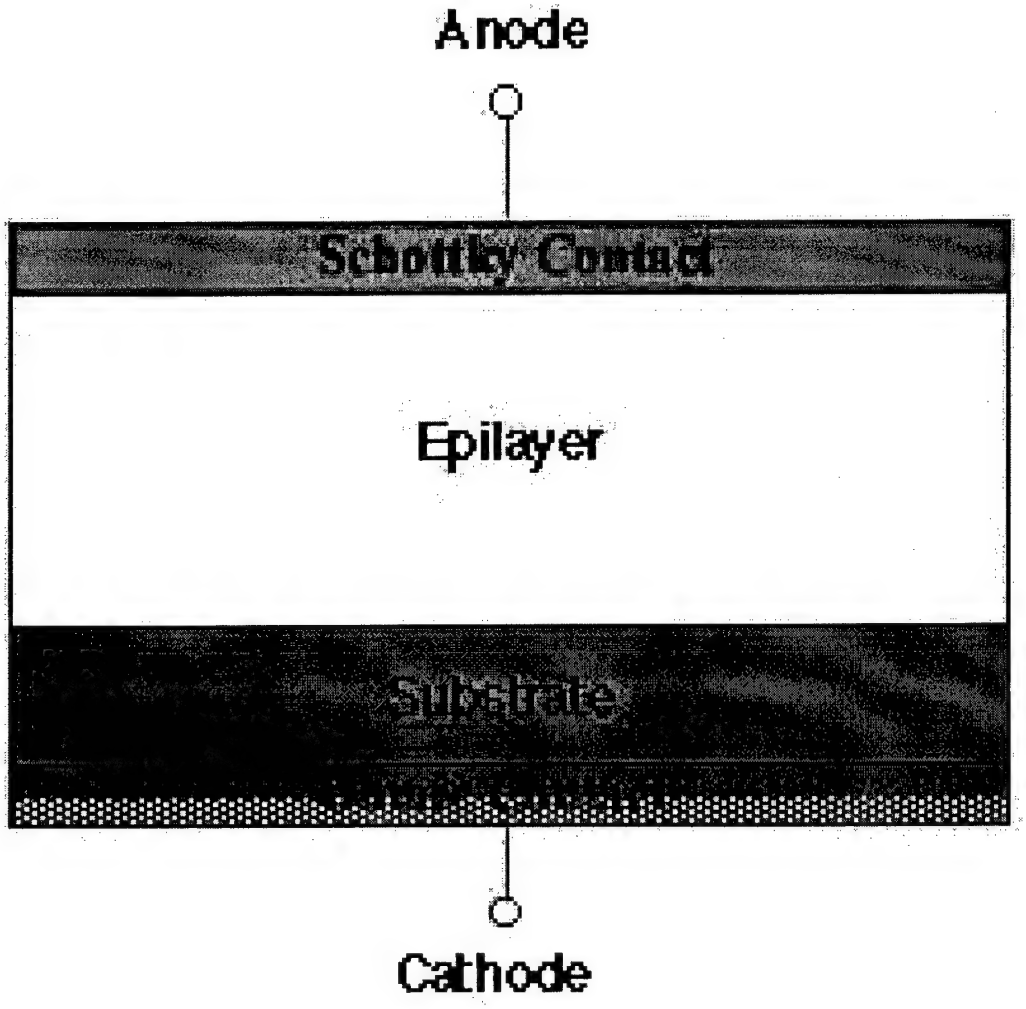

Figure 1.2: Cross section of SiC SBD

CHAPTER II

THEORY OF SCHOTTKY BARRIER DIODES

As mentioned in Chapter One, the Schottky barrier diode has become the device of choice for demanding switching applications where its alternative, the p-n diode, is not the ideal device. In theory, the SBD resembles a p-n junction diode with the p-type semiconductor replaced by the metal contact; hence it is a unipolar device [20]. This chapter presents the theory of operation of the SBD. First, the energy band diagram of the metal-semiconductor contact will be presented in detail. The band diagram description is one means to illustrate the device physics. Presented next is a description of the SBD in operation, which consists of the diode characteristics under forward and reverse bias. This section will begin with a description of the ideal characteristics observed in both forward and reverse bias followed by the non-ideal characteristics. Then, a discussion of anomalous operation will be presented to facilitate the understanding of a real device. Finally, practical design considerations are given to conclude this chapter. Throughout the chapter, important parameters of the SBD will be defined. Later, in Chapter Three, the testing used to extract these parameters will be discussed in further detail.

Basic Theory of Operation

To begin the discussion of the theory of operation of the SBD, the energy band diagram of the metal and semiconductor in isolation is presented in figure 2.1 [20]. This figure shows the vacuum energy level, E_0, of equal value for both materials. E_0 is defined as the minimum energy level of a completely free electron or an isolated electron in vacuum [1]. The figure also shows the work functions of the metal, Φ_M, and the semiconductor, Φ_S. Work functions of materials are defined as the energy difference from the vacuum energy to the Fermi energy level, E_F [20]. They are defined in terms of the energy unit of the electron, i.e., electron-volts (eV). (When discussing the work function as a potential, the symbol ϕ is used and is defined as the energy Φ divided by the electron charge, q, which has the units of Volts [21]). The metal's work function is directly related to the type of metal used for the SBD [20]. Notice, for this case, the work function of the semiconductor (Φ_S) is less than the work function of the metal. Φ_S is dependent on the doping concentration of the semiconductor, but the energy difference between the vacuum level and the conduction band, E_C, is a fundamental constant of the semiconductor. This difference is defined as the electron affinity, χ. Now, with the use of the electron affinity, one of the most important parameters associated with SBD's, the Schottky barrier height, may be realized. The barrier height ,Φ_B, as seen in figure 2.2, is defined by the difference in the metal work function and the electron affinity when the metal and semiconductor have come into perfect contact as shown in equation 2.1.

$$\Phi_B = \Phi_M - \chi \tag{2.1}$$

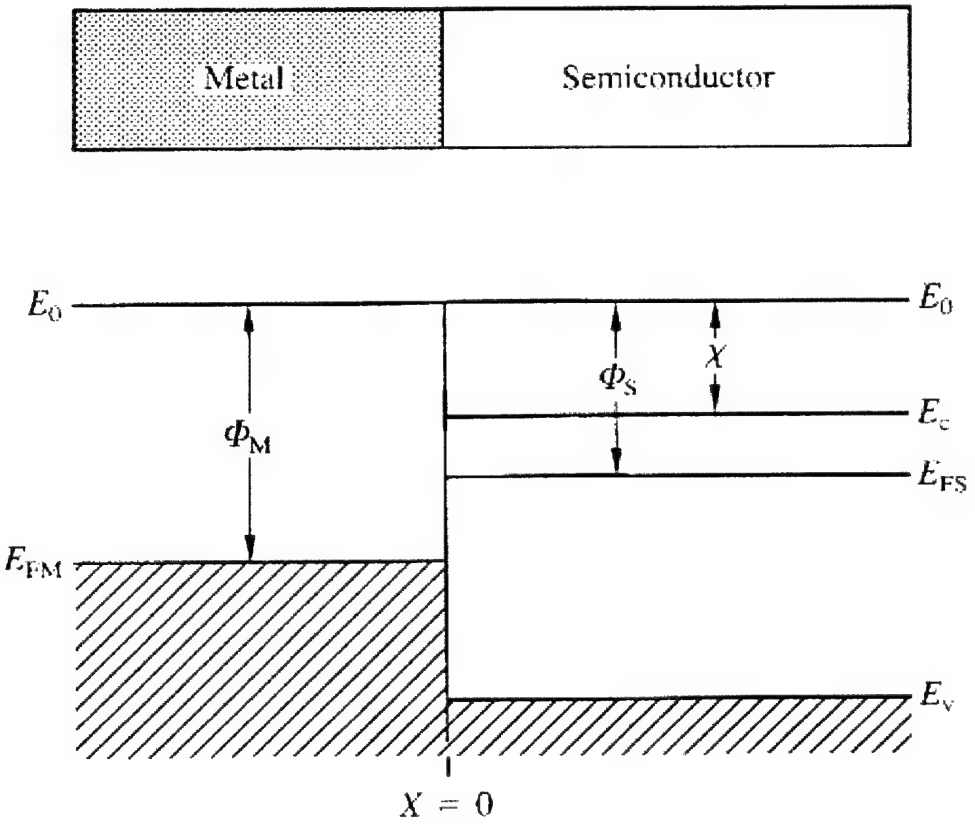

Figure 2.1: Energy band diagram of isolated metal and semiconductor regions (from [20])

The barrier height is independent of the semiconductor doping density and therefore easy to vary by selecting the proper metal with an appropriate work function [21]. By joining the Fermi levels of the metal and the semiconductor, the next figure shows the metal-semiconductor system in thermal equilibrium, which demonstrates all of the work functions and complete energy band diagram of the SBD.

When the metal and semiconductor act as a single system, the electrons in higher energy levels in the semiconductor move into the metal until the average electron energies are equal [1]. When the electron transfer is complete, the SBD has come to thermal equilibrium (TE). Thermal Equilibrium is shown in figure 2.2. In TE, it is easy to see that the Schottky barrier is a potential barrier that is seen by an electron with energy equal to the Fermi level, E_F [20]. Based on the resulting band bending, a built in potential ,V_{bi}, defined by the following equation, is also present in the metal-semiconductor band diagram of figure 2.2 [1].

$$qV_{bi} = q\phi_M - q\phi_S \tag{2.2}$$

Now that the basic definitions have been presented, ideal SBD electrostatics can now be explained so that the SBD under external bias can be understood. To do so, the charge density (ρ), electric field (E), and electrostatic potential (V) will be used [20]. Figure 2.3 shows the variation of ρ, E, and V as a function of distance, x, defined from the metal-semiconductor junction (i.e., x=0) where x_n is defined as the edge of the depletion region in the n-type semiconductor, that was created by the movement of electrons into the metal [1]. The remaining ions in the depletion region create an electric field that is associated with the appearance of a potential difference between the metal and the semiconductor bulk [1].

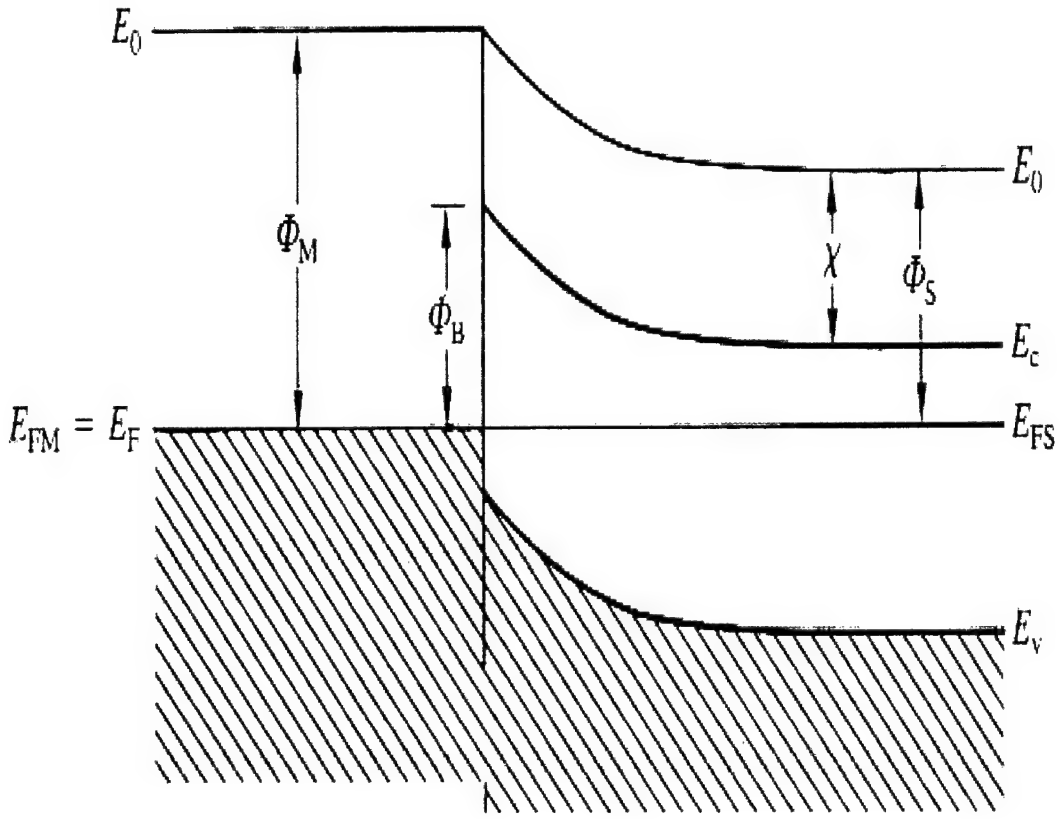

Figure 2.2: Thermal equilibrium energy band diagram for the Schottky diode after metal-semiconductor contact has been made (from [20]).

By defining Q_S and Q_M as the charge per unit area of the semiconductor and metal respectively, charge neutrality can be used to describe the metal-semiconductor junction charge distribution as follows [20]:

$$Q_S = qN_D x_n = Q_M \tag{2.3}$$

The concept of charge neutrality described by equation 2.3 is shown in figure 2.3 b) for reference. The electric field as a function of x is also defined as

$$\overline{E}(x) = \frac{-qN_D}{K_S \varepsilon_0}(x_n - x) * \hat{a}_x \tag{2.4}$$

where Ks is the dielectric constant of the semiconductor. The electric field at the metal semiconductor junction is shown in the diagram of 2.3 c). Since the electric field and potential are related by $\boldsymbol{E} = -\nabla V$, and the built-in potential plotted versus x as shown in figure 2.3 d) and given by

$$V(x) = V_{bi} - \frac{qN_D}{2K_S \varepsilon_0}(x_n - x)^2 \tag{2.5}$$

Now that the electrostatic variables for the SBD have been defined in thermal equilibrium, it is logical to discuss the SBD under non-thermal equilibrium conditions (i.e. active bias).

Applied Bias

Under electrical bias, the SBD behaves similarly to the pn junction diode. The applied voltage, V_A, reduces the energy barrier in the depletion layer to $q(V_{bi}-V_A)$ which enables electrons from the semiconductor to overcome more easily the Schottky barrier and move into the metal under forward bias [1].

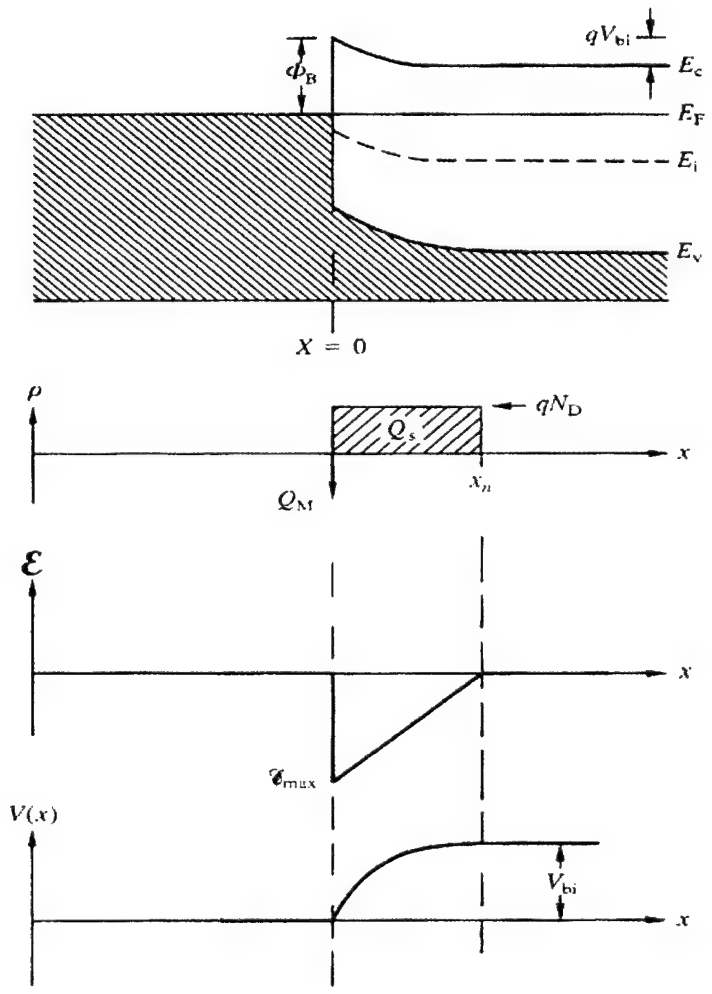

Figure 2.3: Energy band diagram, ρ vs. x, E vs. x, V vs. x (from [20])

Under reverse bias the barrier is increased by qVA, which means that the depletion region x_n increases. Under reverse bias the current flowing is very small due to the large increase in the potential barrier [20]. However, it must be noted that, to the first order, the barrier height Φ_B does not change with applied bias. This can be seen in figure 2.4. Current may flow in both directions: J_{MS} is the current flow from the metal to the semiconductor and the barrier to current flow is $q\phi_B$. J_{SM} is the current flow in the opposite direction with a barrier of $q(V_{bi} - V_A)$. Note that the barrier to the current flow under reverse bias (J_{MS}) is independent of bias, while the current flow under forward bias(J_{SM}) is a strong function of bias. In order to derive the ideal current equation for the SBD, it is important to understand the significance of the Fermi-Dirac function.

The Fermi function definition states that the probability that an electron will have energy, E, is

$$f = \frac{1}{1 + e^{\frac{E - E_F}{kT}}} \tag{2.6}$$

where k is Boltzmann's constant, and T is the temperature [1]. For energies greater than $3kT + E_F$, the Fermi-Dirac distribution can be approximated as follows:

$$f \approx e^{\frac{-(E - E_F)}{kT}} \tag{2.7}$$

This implies that for Φ_B greater than 3kT, the number of electrons with energies above the barrier decreases exponentially with increasing electron energy [20]. In other words, the larger the barrier height, the lower the leakage current, and the carrier flux will decrease exponentially.

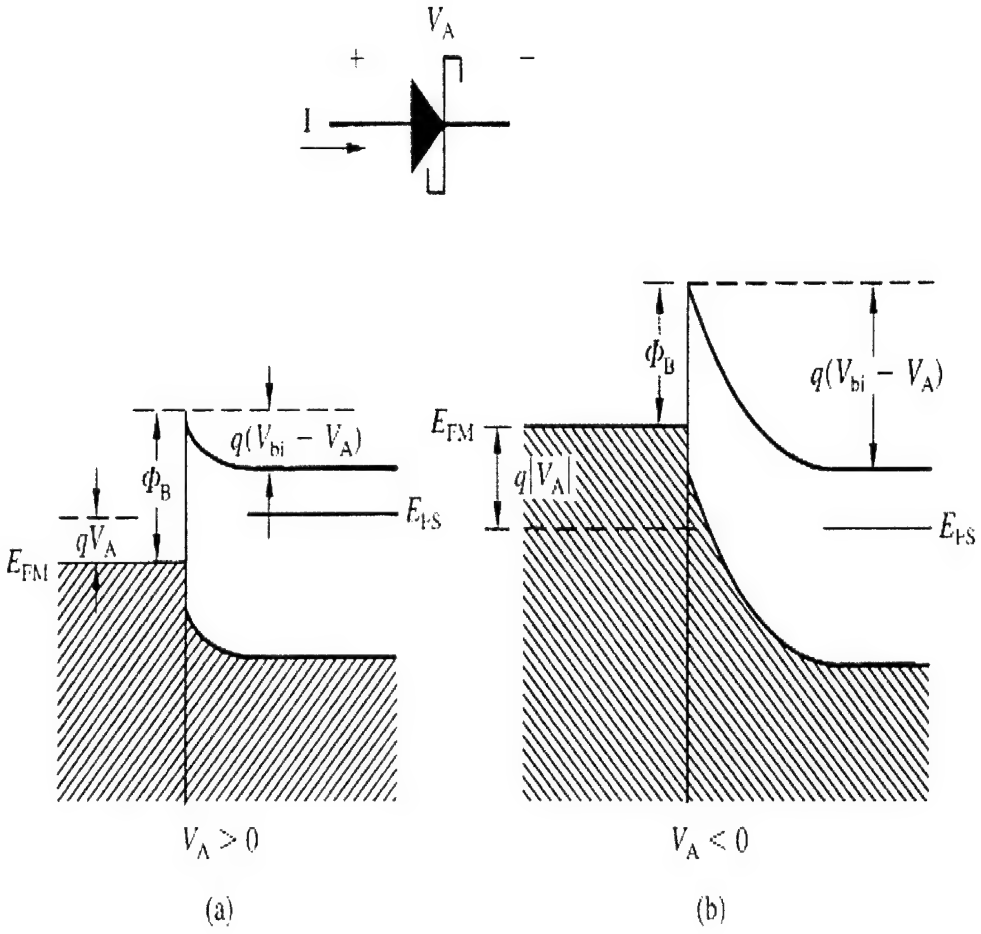

Figure 2.4: Energy band diagram for an SBD under active bias. (a) Forward bias and (b) reverse bias conditions (from [20]).

To begin the discussion of the SBD current equations, a brief discussion of equilibrium, or $V_A=0$, is needed. As mentioned earlier, the electrons at the edge of the conduction band in the semiconductor see a built-in potential barrier. As the Fermi function suggests, the number of electrons with energies greater than E_C+qV_{bi} decreases exponentially with increasing energy. So, in thermal equilibrium, the number of electrons traversing from the metal to the semiconductor must equal the number of electrons traversing from semiconductor to the metal, i.e. $J_{S-M} = J_{M-S}$ [20]. These current densities are well known as drift and diffusion currents respectively. This electron movement can be seen in figure 2.5. The continuum of electron energy states can be modeled as a single level with density N_C at the conduction band edge E_C. Now, in order to compute the concentration of free electrons, n, simply multiply N_C with the Fermi function to get

$$n = \frac{N_C}{e^{\frac{E_C - E_F}{kT}}} \tag{2.8}$$

For the concentration of free electrons at the metal-semiconductor junction, n_s, the energy difference from E_F to E_C is the barrier height, which yields the following [20]:

$$n_s = \frac{N_C}{e^{\frac{\Phi_B}{kT}}} \tag{2.9}$$

From figure 2.5, it can be seen that the barrier height can be defined as the built in voltage added to the difference of the conduction band and the Fermi level. Substituting this into equation 2.9 gives the following:

$$n_s = N_C e^{\frac{-(E_C - E_{FS})}{kT}} e^{\frac{-qV_{bi}}{kT}} \tag{2.10}$$

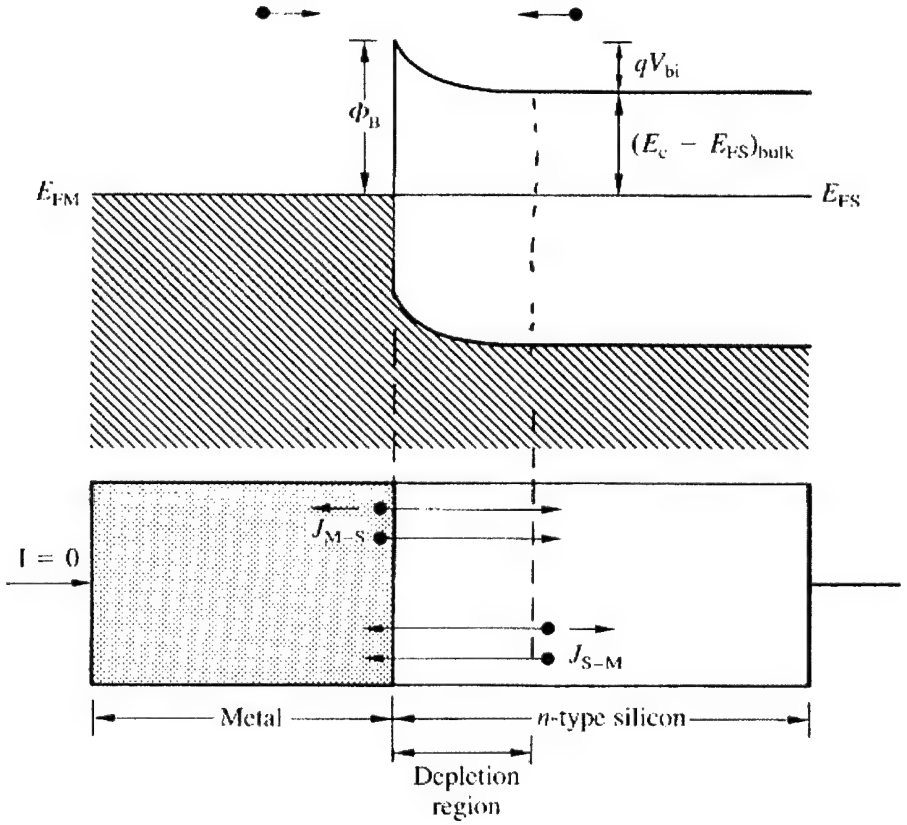

Figure 2.5: Schottky barrier height and the corresponding drift current, J_{MS}, and diffusion current, J_{SM} (from [20])

For a semiconductor containing fully ionized dopant, $n = N_D$ so that

$$n_s = N_D e^{\frac{-qV_{bi}}{kT}} \tag{2.11}$$

which yields the following equation for diffusion current and drift current in TE:

$$J_{M-S} = -K_1 N_D e^{\frac{-qV_{bi}}{kT}} = -K_1 N_C e^{\frac{-\Phi_B}{kT}} = -J_{S-M} \tag{2.12}$$

where K_1 is a proportionality constant [19].

The ideal forward bias characteristics may now be discussed. Forward bias is the condition when V_A is greater than zero. As mentioned earlier, with a positive V_A the electrons can easily overcome the potential barrier allowing current to flow. A drift current still exists which implies that electrons still flow from the metal to the semiconductor, but this current is overcome by the diffusion current which allows the electrons to pass from the semiconductor to the metal [1]. The diffusion current in forward bias is given by the following equation:

$$J_{S-M} = K_1 N_D e^{-\frac{q(Vbi-VA)}{kT}} \tag{2.13}$$

However, in order to account for the total current, the drift current must also be added to the above equation.

$$J_{TOT} = K_1 N_D e^{-\frac{q(Vbi)}{kT}} [e^{\frac{q(V_A)}{kT}} - 1] = K_1 N_C e^{\frac{(-\Phi_B)}{kT}} [e^{\frac{q(V_A)}{kT}} - 1] \tag{2.14}$$

By equating the reverse saturation current, J_0, to the product of the proportionality constant, the effective density of states and the exponential term with the barrier height, the final expression for the ideal forward bias current can be realized [20]:

$$J_{FB} = J_0 [e^{\frac{q(V_A)}{kT}} - 1] \tag{2.15}$$

Next, the SBD ideal reverse bias current can be derived. Reverse bias is defined as having V_A less than Zero [1]. In reverse bias, the diffusion current is negligible while the drift current becomes dominant due to the fact that this current is solely dependent on the unchanging barrier height [20]. The drift current can be visualized as the amount of electrons that can overcome the barrier height and is therefore proportional to $\exp(\Phi_B/kT)$. Since the reverse bias current can be seen ideally as merely the drift current supplied by the electrons moving from the metal to the semiconductor, it can be defined as the reverse saturation current mentioned earlier [1].

$$J_{TOT} = -J_0 = -K_1 N_C e^{\frac{-\Phi_B}{kT}} \tag{2.16}$$

Now that the SBD current-voltage behavior under active bias has been developed, a key theoretical consideration must be discussed.

Non-ideal Operation

Up until this point the ideal operation of the SBD has been discussed. Now, the nonidealities will be discussed for a deeper understanding of the operation of the SiC SBD, which is the subject of this thesis research. The main causes of the non-ideal operation can be attributed to the yield considerations mentioned above, but there are other "naturally" occurring events that take place in the SBD such as reverse bias breakdown, thermionic emission, thermionic field emission and field emission. Two more non-ideal characteristics observed in forward bias operation will further impact the ideal diode equation of 2.16.

Although many diodes are fabricated for the purpose of conducting in reverse breakdown (e.g., Zener diode), reverse breakdown is not an "ideal" mode of operation.

Two main methods exist for causing a diode to enter reverse breakdown. The first is avalanche breakdown, which is described as an electron-hole generation process that occurs when a sufficiently large electric field has been induced in the depletion layer and impact ionization occurs [1]. Once this field grows strong enough, an avalanche process generates an enormous amount of free carriers, which in turn produces a large increase in the negative current. The next method for a diode to enter reverse breakdown is the tunneling effect, which is the mode of operation for Zener diodes [1]. Tunneling current is the main non-ideal mechanism that takes place in SBD's. Tunneling current occurs between two dissimilar materials with the application of high electric fields [22]. The tunneling effect occurs when the depletion width grows and the distance between energy bands decreases, which allows electrons to defeat the barrier by "tunneling" through rather than going over it.

Three types of conduction mechanisms exist in SBD's that are directly related to the doping density (figure 2.6) [21], each of which add parameters to the ideal diode equation 2.16. The first mechanism is thermionic emission. Thermionic emission is a situation where the doping density is low in which case only the thermally excited electrons can pass over the energy barrier allowing current to flow. Its equation consists of replacing the constant K and the effective density of states in the reverse saturation current equation with the Richardson coefficient, A* (for 4H-SiC = 146 A-cm^{-2}-K^{-2}) multiplied by the square of the temperature, which yields

$$J_0 = A^* T^2 e^{-\frac{\Phi_B}{kT}} \tag{2.17}$$

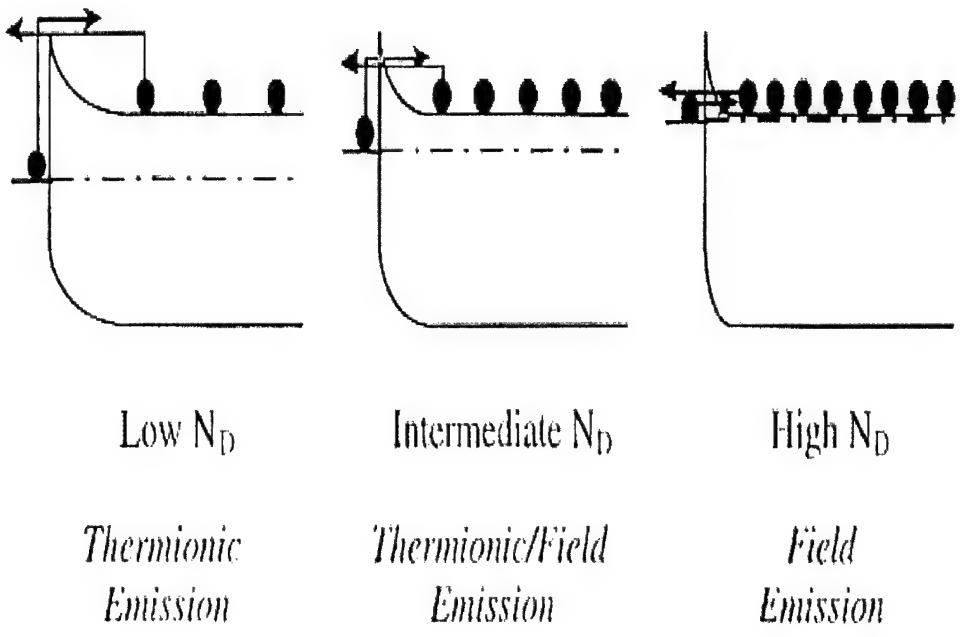

Figure 2.6: Reverse bias electron flow (from [21]) in a SBD caused by non-ideal electron transport mechanisms.

Next is thermionic field emission, which is observed in devices with intermediate doping. This is the first mechanism of tunneling, and it is the most commonly found mode of operation in SiC SBD's [2]. In this state, the thermally excited electrons have reached an energy where they can tunnel through the barrier, but an electric field is necessary to assist the carriers by narrowing the barrier. Finally, for high doping densities, the barrier is found to be sufficiently narrow at or near the bottom of the conduction band. In this situation, the electrons have no problem tunneling through the energy band gap from one side of the diode to the other. This is known as field emission [21]. Thermionic emission and field emission contribution to the ideal diode equation add the tunneling probability formula, which will not be presented in this work.

Crofton and Sriram observed that field emission and thermionic field emission could take place at different voltages in the SBD [2]. They concluded that in SiC simply fitting the thermionic emission equation to the reverse bias curve would provide many orders of magnitude error due to the fact that it does not take into account the tunneling phenomena. Instead, they used a method of calculating the tunneling probability through a parabolic Schottky barrier for a large range of electric fields, temperatures, and barrier heights.

Finally, to complete the discussion of the non-ideal operation description of the SBD, a brief discussion of the on-state resistance and the ideality factor is in order. The effects of these two deviations from the ideal are mainly seen in forward bias [20]. The ideality factor is an empirical term, n, which is added to the exponential term of the forward bias current equation as follows:

$$J_{FB} = J_0[e^{\frac{q(V_A)}{nkT}} - 1] \tag{2.18}$$

Typical values for the SBD's ideality factor range between 1 and 2. The specific on resistance of the diode, R_{ON}, is seen at higher levels of current when the series resistance of the device takes over and provides an additional voltage drop [8]. This forward voltage drop is given by

$$V_F = \frac{nkT}{q}\ln(J_{FB}\ A^*T^2) + n\Phi_B + R_{ON}J_{FB} \tag{2.19}$$

The reason that a low forward voltage drop is desirable is that it minimizes unwanted power consumption.

Anomalous Operation

Anomalous operation of the SBD's in this work is considered to be leakage currents that show a significant voltage dependence. They include the effects of material defects, Schottky barrier lowering and edge termination leakage currents.

As mentioned in the previous investigations section, Neudeck has investigated extensively the effects of material defects on SiC devices [16, 18]. His diodes consistently reported higher leakage on larger area devices. This suggests that the larger area devices are covering more of the defects in the substrate and epilayer than that of the smaller devices. In his investigations, he closely examined the concentrations of elementary 1C screw dislocations, micropipes, growth pits and other material defects and successfully presented that the devices located in the higher concentration areas of those defects exhibited higher leakage and lower reverse bias breakdown [16, 18].

Another anomalous contribution to reverse leakage current that is not easily predicted is Schottky barrier lowering ($q\Delta\phi$). This is an effect that was first documented during Walter Schottky's electron emission studies [22]. This mechanism is again seen in reverse bias and can be attributed to a gradual increase in leakage current. The effective barrier height is found by subtracting the barrier lowering term from the barrier height. The barrier lowering term is approximated as

$$q\Delta\phi = \sqrt{\frac{q^3 \overline{E}}{4\pi\varepsilon_s}} \tag{2.20}$$

where ε_S is the permitivity of the semiconductor and the electric field is given at the metal-semiconductor interface [22]. A more detailed model of this effect is realized by taking into account the non-uniform electric field.

The final contribution to unwanted, unpredictable leakage current comes from the various types of edge terminations mentioned in the investigations section. The general idea behind edge terminations is to relieve the electric field stress beneath the Schottky contact by creating a more even distribution of equipotential lines and therefore increasing performance. The major side effect of this is that the spreading of the field lines tends to draw current over the resistive surface of the termination [12].

A model demonstrating the various regimes of the SiC SBD is found in figure 2.7. This figure shows the various contributions of each reverse bias mechanism and what regime the actual diode typically follows. As seen in the diagram, a typical SiC SBD begins by following the thermionic field emission model, and then either follows the field emission model briefly or moves directly into anomalous operation. The conclusion of the typical operation is when the diode finally snaps into avalanche breakdown.

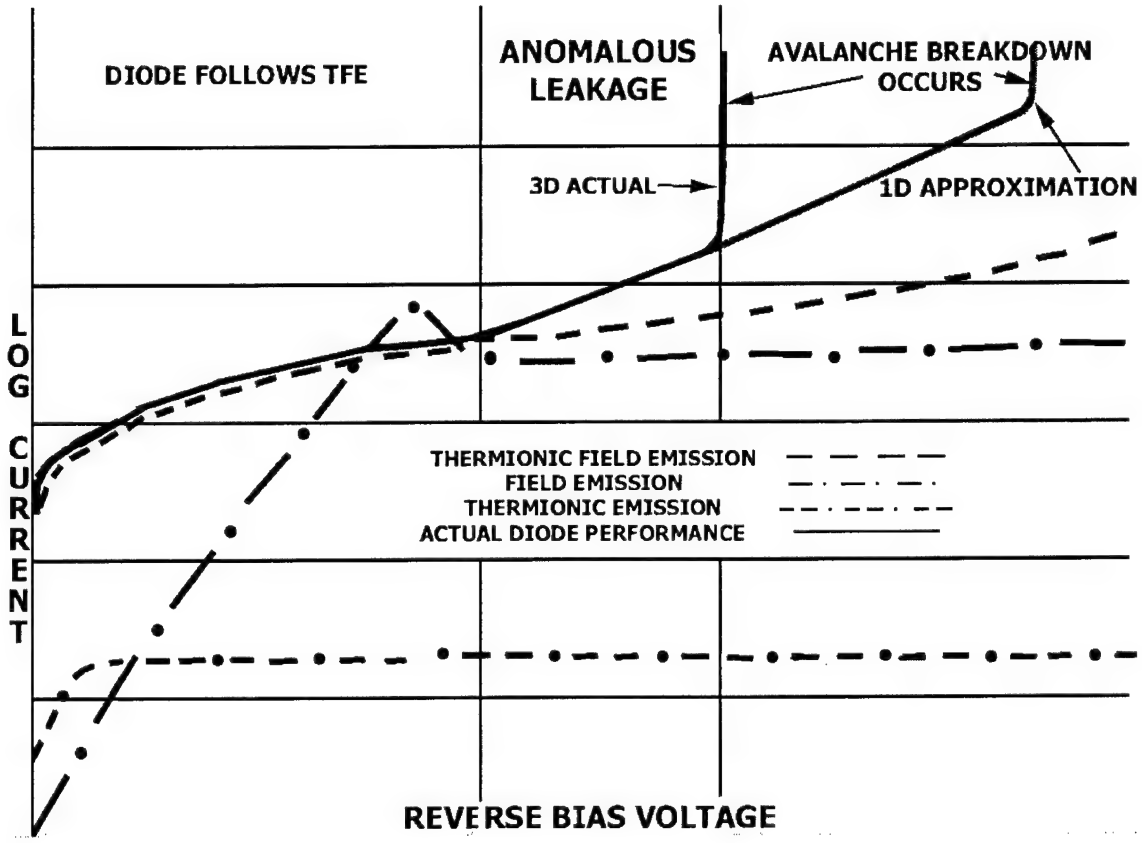

Figure 2.7: Typical SiC SBD reverse bias performance compared with theoretical performance regimes.

Shown in the diagram is the simulated 1D approximation of reverse bias breakdown that can be found by using the equations mentioned in this chapter. Also shown is the more likely 2D breakdown. It must be noted that at no time does a SiC SBD follow the ideal thermionic emission theory, nor is actual avalanche breakdown observed at the theoretical limit, but at some fraction of the 1D limit determined by the design of the edge termination.

Practical Design Considerations

In the SBD design process, many important decisions must be made to assemble the materials into a device that meets the desired electrical characteristics. The main design variables that affect the SBD performance are the contact metal work functions, the epilayer doping, the epilayer thickness and the selection of an edge termination technique to suppress surface breakdown [14]. There is also the question of the ohmic contact to the semiconductor which has an impact on device performance.

The first parameter to be discussed for a vertical SBD is that of the ohmic contact. The ohmic contact is commonly referred to as the backside contact. It provides a contact area for the cathode. In the selection of a metal for this contact, it is important to pick a metal with a low work function and low series resistance [23]. However, in order to prevent the ohmic contact from becoming an extra, unwanted Schottky contact, the metal must alloy well to the substrate. This is done by a process called the contact anneal which is a high temperature annealing process. Table 2.1 lists different types of metal and their properties following the annealing process to 4H-SiC. Since the ohmic contact anneal is the highest temperature process (after epilayer growth), it must be done prior to Schottky contact formation.

Table 2.1

Table of Ohmic Contact Properties for 4H-SiC (from [23])

Metallization	Annealing °C	SiC Carrier Concen. (cm^{-3})	SiC Type	ρc at 300 K (Ω/cm^2)	ρc Measurement Method
Ni	1000-1200, 1min	3.2×10^{17}-1.4×10^{18}	N	1.3×10^{-5}-3.6×10^{-6}	TLM
Ni	950-1000	2×10^{18}-2×10^{19}	N	4×10^{-4}-10^{-6}	TLM
Mo	950-1000	2×10^{18}-2×10^{19}	N	4×10^{-4}-10^{-5}	TLM
Ni, Ni/W, Ni/Ti/W, Ni/Cr/W	1000-1050, 5-10min	10^{17}- 10^{18}	N	10^{-3}-10^{-6}	TLM
Cr/W, Cr/Mo/W	1000-1050, 5-10min	10^{17}- 10^{18}	N	10^{-2}-10^{-4}	TLM
Al/Ni/Al	1000, 5min	10^{19}	N	1.8×10^{-5}	XPS

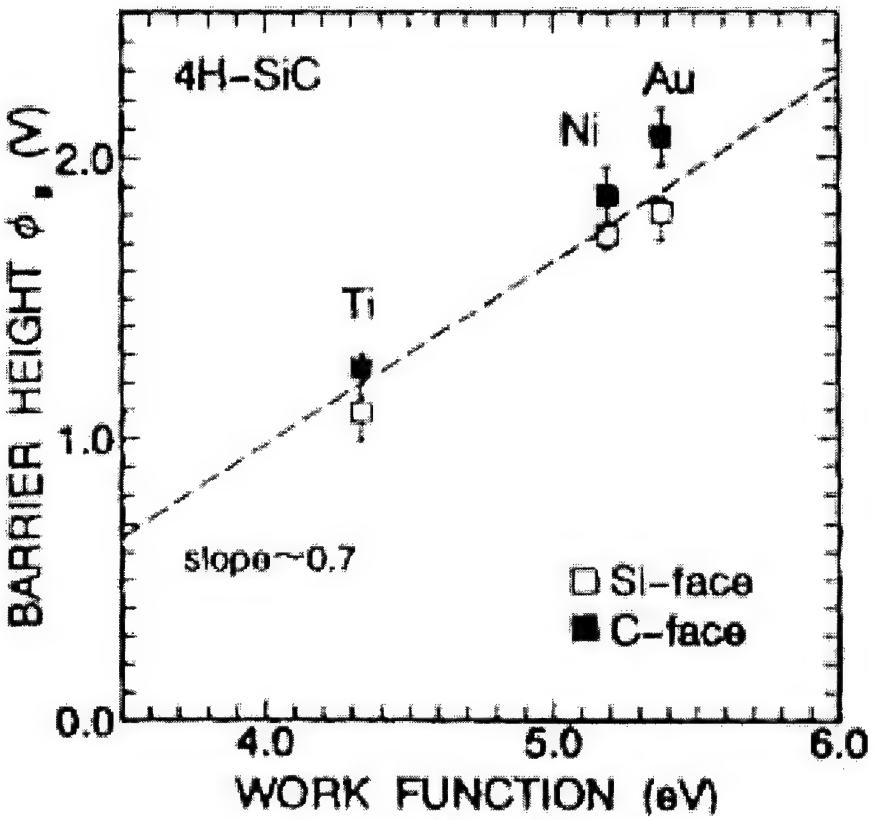

Figure 2.8: Schottky barrier height as a function of the metal work function for n-type 4H-SiC material (from [23]).

Next is the selection of the topside Schottky contact. When selecting this metal, again it is important to pick a proper work function because of the close relationship between the metal work function and the Schottky barrier height. Figure 2.8 shows the relationship between the resulting barrier heights vs. titanium, nickel, and silver work functions [23]. Also, Table 2.2 shows a comparison of several Schottky metals and their properties. The next step in the design process is the selection of the epilayer thickness and doping density. These two properties directly determine the target reverse breakdown voltage [14]. The doping density can be related to this voltage as

$$N_D = \frac{\varepsilon_S E_{CR}^2}{2qV_{BR}} \tag{2.21}$$

where E_{CR} is the critical field of the semiconductor and V_{BR} is the reverse breakdown voltage. The thickness of the epilayer grown also is critical in determining the reverse breakdown voltage [14]. It is defined as follows:

$$t_{epi} = \frac{2V_{BR}}{E_{CR}} \tag{2.22}$$

These two factors determine the avalanche breakdown voltage, but as mentioned earlier, one of the major components of reverse leakage current is due to tunneling seen at higher levels of doping. In the selection of a low on-state resistance and low forward drop, the epilayer thickness also is a critical design parameter. The following equation relates the resistance to the epilayer thickness:

$$R_{ON} = \frac{t_{epi}}{q\mu_n N_D} \tag{2.23}$$

Table 2.2

Table of Schottky contact properties for 4H-SiC (from [23])

Metallization	Carrier Concentration (cm^{-3})	SiC type	Resulting Barrier Height (eV)	Barrier Height Measurement Method
Au	$5x10^{15}$	N	1.73-1.8	IV, CV
Ni	$5x10^{15}$	N	1.6-1.7	IV, CV
Ni	$6x10^{15}$	N	1.67	IV
Pt	$6x10^{15}$	N	1.31	IV
Ti	$5x10^{15}$	N	1.1-1.15	IV, CV
Ti	$1x10^{16}$	N	0.99	IV

The next design parameter that must be considered is the SBD's edge termination The reverse bias breakdown voltage of rectifiers can be drastically reduced by the occurrence of high electric fields either from the interior portion of the device or at the device's edge [12, 21]. However, by selecting the proper edge termination technique, the breakdown voltage along with the drift region, which affects the forward bias characteristics, can be optimized for much improved performance. MEDICI ™ simulations are often performed to simulate the field stress throughout the device [14].

As mentioned in the previous section, there are many termination choices. The most popular is implanting a p-type ring around the anode and then annealing the devices to both activate the implant and reduce any damage that may have occurred in the implant process [23]. This termination method relies on the ability to introduce charge at the surface near the metal-semiconductor junction by using ion-implantation [24]. The precision of the implant doping directly controls the effectiveness of the termination. If the doping is too low, the implant has literally no effect on the device and the field crowding still occurs beneath the SBD. If the doping is too high, all of the crowding occurs at the outer edge of the implant. Therefore, it is essential that the implant be precisely doped such that the implant region is completely depleted under reverse bias. An alternative is to use argon damage implants, which acts only as a neutral resistive layer to suppress the field crowding [25]. In Cree's research on various types of edge terminations, they did find that the single floating ring ion implant was the most effective termination method [15]. Those devices demonstrated a higher yield and higher breakdown voltage. Many have stated that using argon implants result in higher leakage

than that of boron or aluminum, but argon makes for an easy and reliable resistive damage implant [10, 11, 12, 22].

Another popular termination is the field plate where the Schottky metal actually overlaps the sides of the device (separated by a field oxide). A field plate overlap results in an expanded depletion region along the surface of the semiconductor below the metal overlap by altering the surface potential [12, 21]. Generally, the field plate is very cheap and easy to fabricate [22, 23]. Investigations have shown that this type of termination results in a lower series resistance (vs. non-terminated devices) due to the increased contact area, which directly improves the forward bias performance [13]. In addition, this type of termination is known for having very low reverse bias leakage currents, but also lower reverse bias breakdown voltages than that of other termination techniques [10, 12, 22].

Finally, the device size is an important design consideration. Size directly affects the breakdown voltage and forward bias current conduction capabilities. It also determines the junction capacitance, which affects the switching speed. As mentioned earlier, material defects cause unwanted leakage current and premature breakdown, especially in SiC SBD's. The general rule of thumb is that larger area contacts results in better forward bias characteristics, but with a lower process and parametric yield, while smaller contacts have a higher yield with better reverse bias characteristics. Many investigations have shown this assumption to be accurate [11, 12, 24].

Two edge terminations (field-plate and argon implant) were simulated in MEDICI™ to pre-determine if the devices designed would be successful. MEDICI™ is a 2D electric field simulation tool that gives the designer an idea of where the field stress

points are in a device that will be the most severe. However, MEDICI™ does not account for anomalous defects and other 3D field effects encountered in real devices. Real devices will display much lower breakdown voltages, which is the reason why this is merely a tool of estimation. The results from the simulations are found in figures 2.9, 2.10, and 2.11. These figures show the potential lines along with the location of the field crowding. The argon implant simulation was visually difficult to distinguish from the non-terminated device due to the fact that approximately one-third of the termination is being employed. However, the results of the simulations show that by adding the argon implanted region the surface field will be reduced by an order of magnitude from the non-terminated device, which gives a theoretical breakdown voltage of ~1400V [25]. The field plate overlap theoretically has a 21% lower breakdown than that of the argon implant devices at 1130V. The electric field manipulation is better illustrated in the field plate simulation in figure 2.11. Now, that the design of the SBD's has been covered, the experimental work of this thesis may be presented.

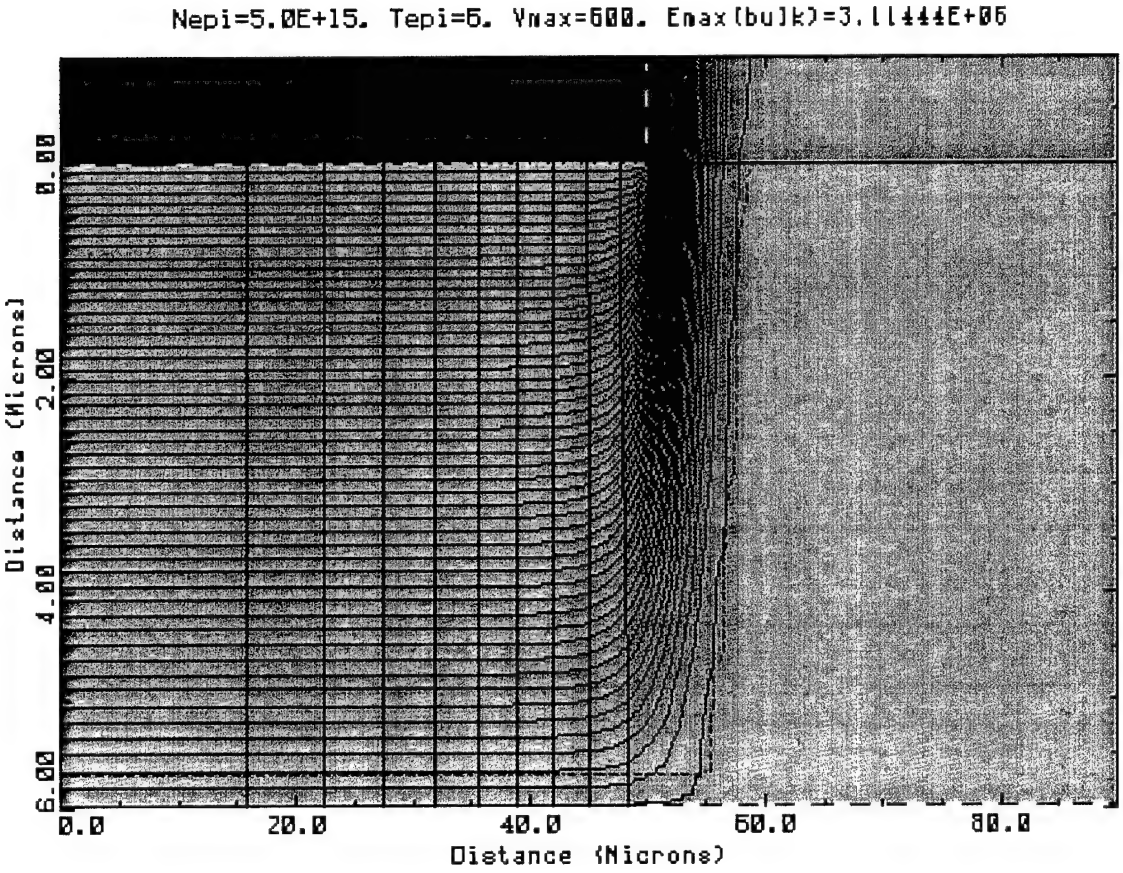

Figure 2.9: MEDICI™ simulation of SBD with no edge termination.

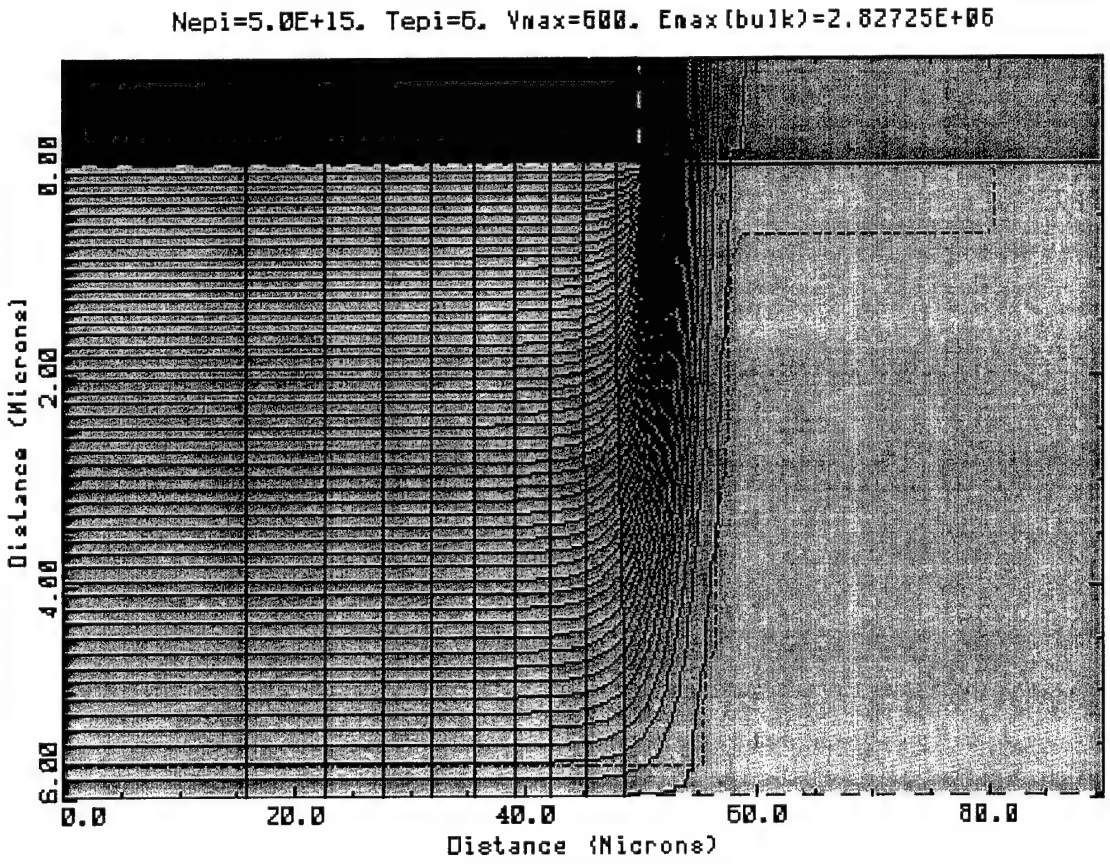

Figure 2.10: MEDICI™ simulation of SBD with argon implant edge termination

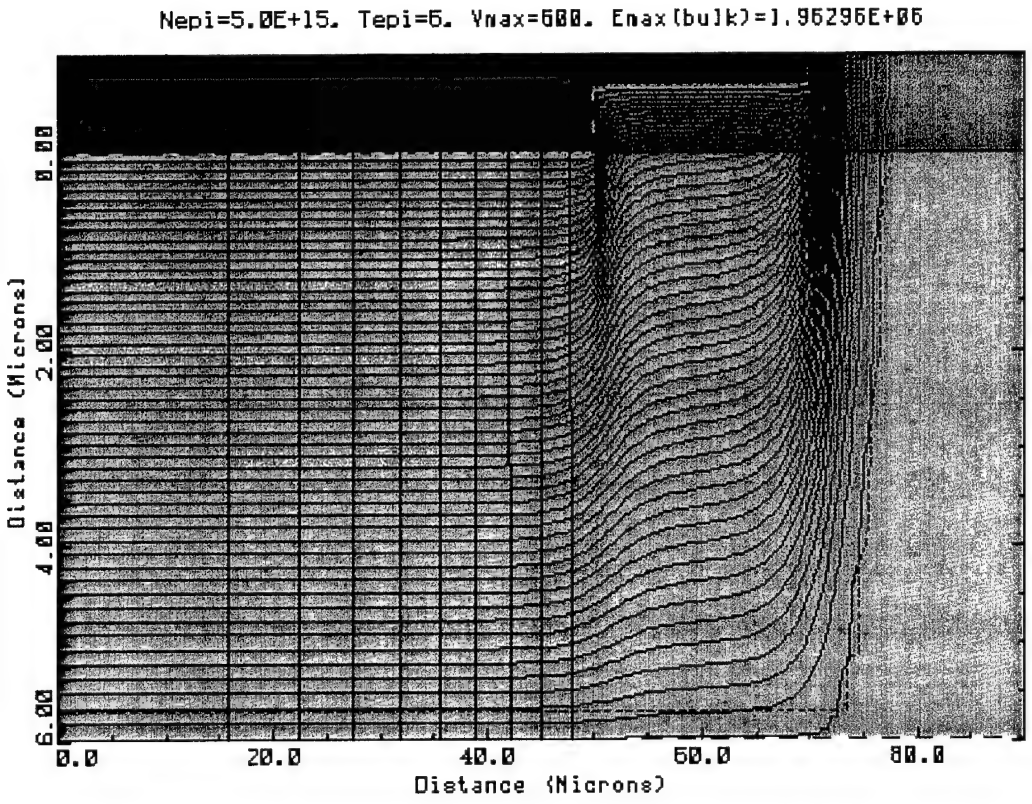

Figure 2.11: MEDICI™ simulation of SBD with field plate overlap edge termination

CHAPTER III

EXPERIMENTAL SETUP

Now that the basics of the SBD have been discussed, the experimental work that this thesis covers, namely the statistical yield model of SiC SBD's, can be explained. This section will begin by discussing in detail the actual fabrication of a lot of 4H-SiC rectifiers. The next section will describe the equipment and testing procedures used and how each piece of equipment assisted in SBD. Then, an explanation of how random sampling was performed to extract yield information will be given. Finally, the chapter will conclude by explaining automated pass/fail testing that was established as part of this work. The explanation of the actual extraction method of the device parameters will be covered in the next chapter.

Fabrication of the SBD's

4H-SiC Schottky barrier diodes were fabricated using 18 research grade wafers from Cree, Inc. Appendix A contains the actual shipping record with electrical characteristics and grade of each wafer. Cold wall chemical vapor deposition (CVD) at 1600 °C using silane, propane, and hydrogen was used for n-type epilayer growth [25]. The net carrier concentration was on the order of 5E15 cm^{-3} with an epilayer thickness ranging between 4 – 10 μm. 1000 Å of nickel was selected for use as the backside ohmic

contact. 800 Å of Titanium was then deposited using an E-beam evaporation for the Schottky contacts. The final metal for both sides consisted of 500 Å of titanium, 1000 Å of nickel, and 2μm of silver. 1mm square shaped (with rounded corners) Schottky contacts were used, including 30 μm on each side for two types of edge terminations. The first edge termination consisted of a selective ring etch and Ar^+ damage implant for half of the devices on the wafer. The other termination was a field plate of an overlap of 20μm over the oxide for the second half of the devices on the wafer. Cross sections of the two SBD's are shown in figures 3.1 and 3.2. The actual devices are found in figures 3.3 and 3.4.

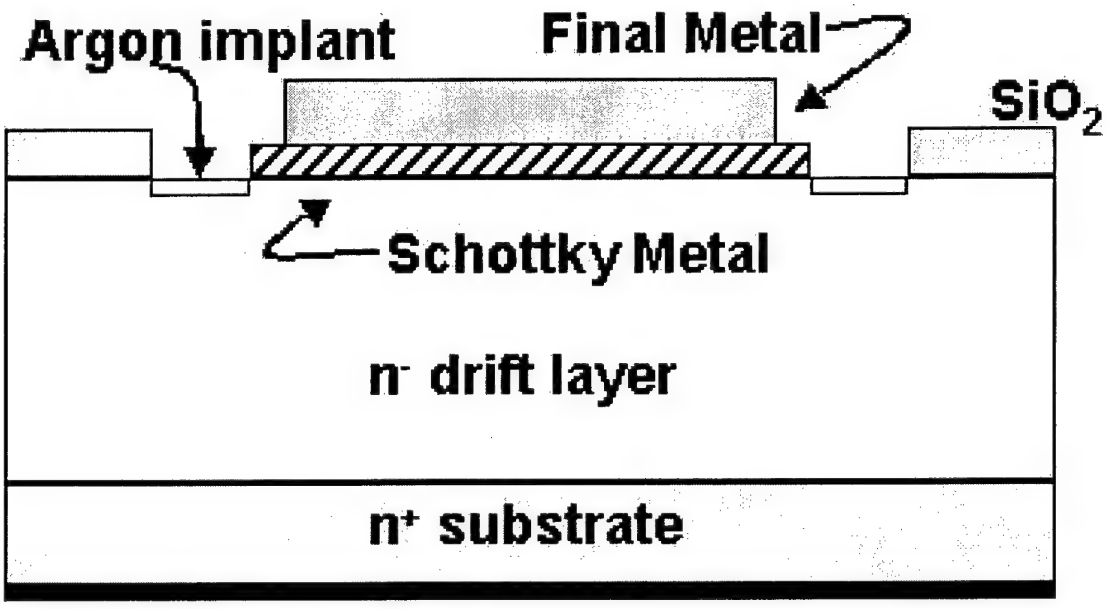

Figure 3.1: Cross section of the SBD's containing argon implant edge termination

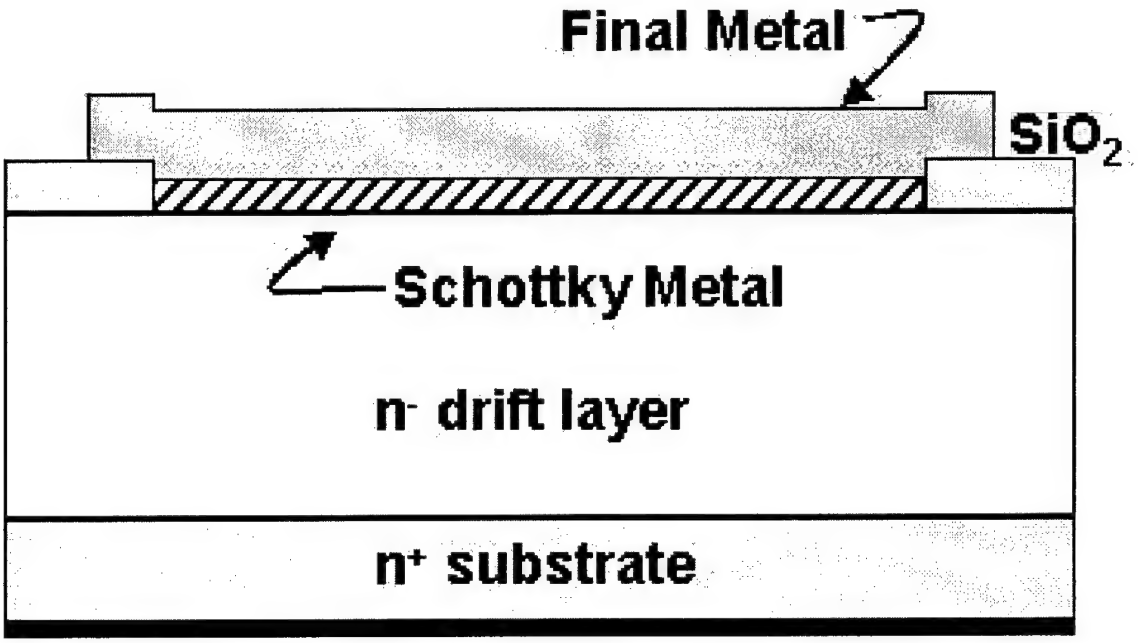

Figure 3.2: Cross section of the SBD's containing field plate overlap edge termination

Equipment Setup

The most important piece of equipment used in the testing of the SBD's was the Wentworth Laboratories model 0-037-1120 Semi-Automatic probe stand. The probe stand is equipped with a Micromanipulator model HSM hot chuck, capable of testing up to 6-inch wafers. A Keithley model 238 (rated at 110V, 1A) source measurement unit (SMU) was used to perform high current and low voltage measurements. Also a Keithley model 237 SMU (rated at 1100V, 100mA) was used to perform high voltage and low current measurements. For detailed leakage current and forward bias analysis, a Hewlett Packard model 4156B parameter analyzer was used. A Keithley model 590 SMU was employed for capacitance-voltage measurements. Although C-V measurements are not

discussed in detail in this work, many others use C-V for parameter extraction rather than I-V. Finally, a Keithley model 707A switch matrix was used in the automation of the setup. The switch matrix's purpose was to enable the use of more than one SMU by isolating the instruments and using solid-state switches to switch between each SMU. This prevents the user from having to make time-consuming manual electrical connections to the probe stand. The automation software used was Labview ™. Labview provided a user-friendly visual programming interface that was easily incorporated with the test instrumentation. Matt Gray performed the programming for the Labview control software under the supervision of Danny Parker [26]. A block diagram of the VASTAC system is found in figure 3.5 where DUT is the device under test.

Random Sample Testing Methodology

Random sample lot testing provides an initial detailed characterization of the devices on each wafer. The random sample test was initially conducted using the Keithley model 237 which was manually controlled by Metrics ICS software ™ through the Keithley switch matrix. An appropriate selection of the sample size is needed to accurately represent the lot of wafers.

In order to represent a population of devices with a variance of 90% and a precision of ± 10% with 99% confidence, a sample size of 59 must be used [27]. However, to correct for the population size of 400 (35mm wafer), the sample size becomes 52. For 750 (50mm wafer) devices, the sample correction is 57 samples [27].

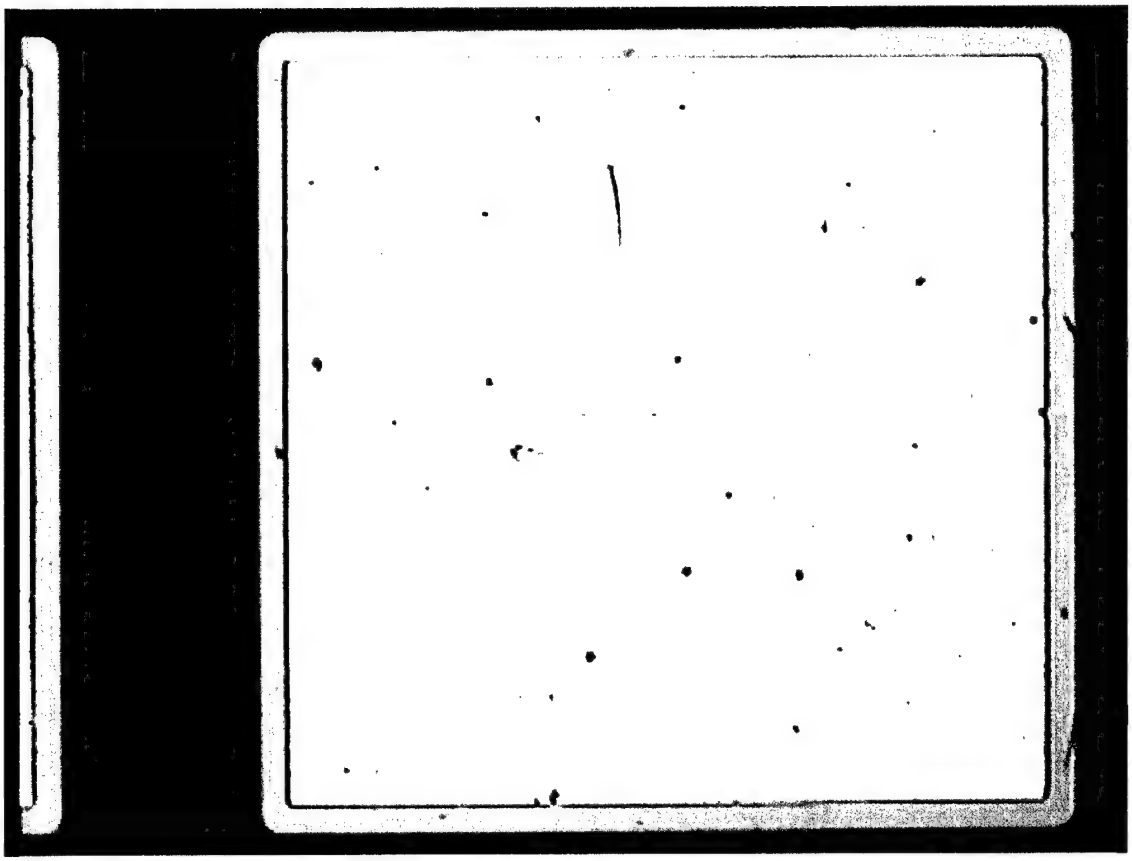

Figure 3.3: SiC SBD with argon implant edge termination

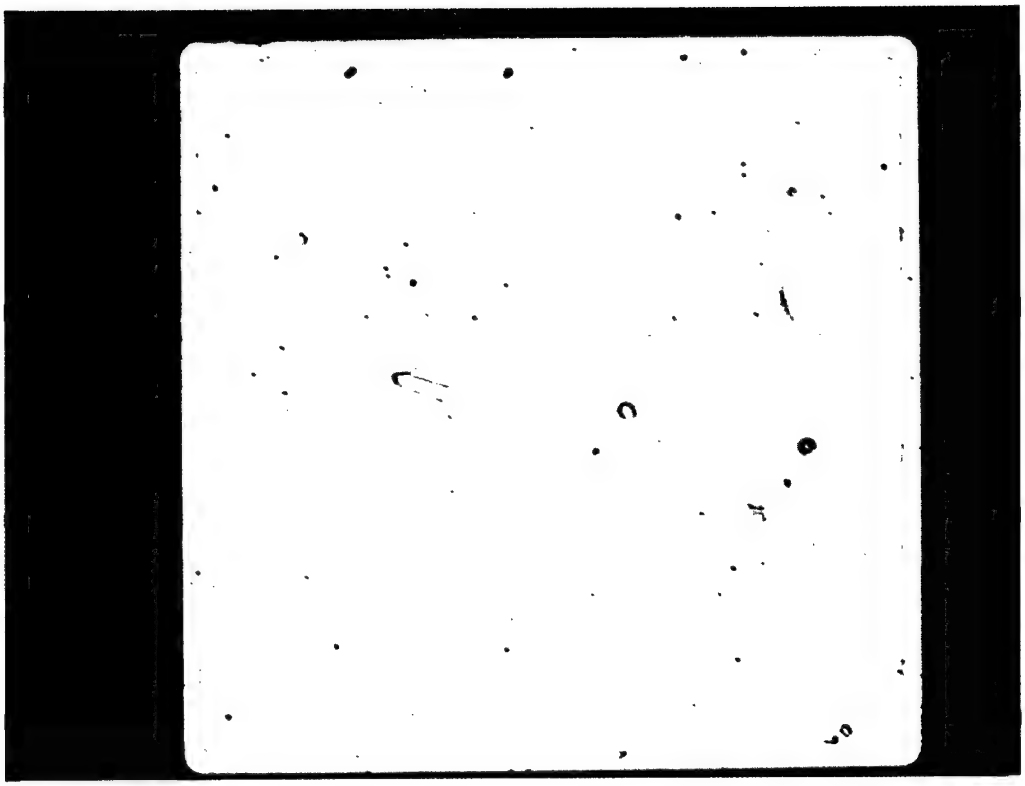

Figure 3.4: SiC SBD with field plate overlap edge termination

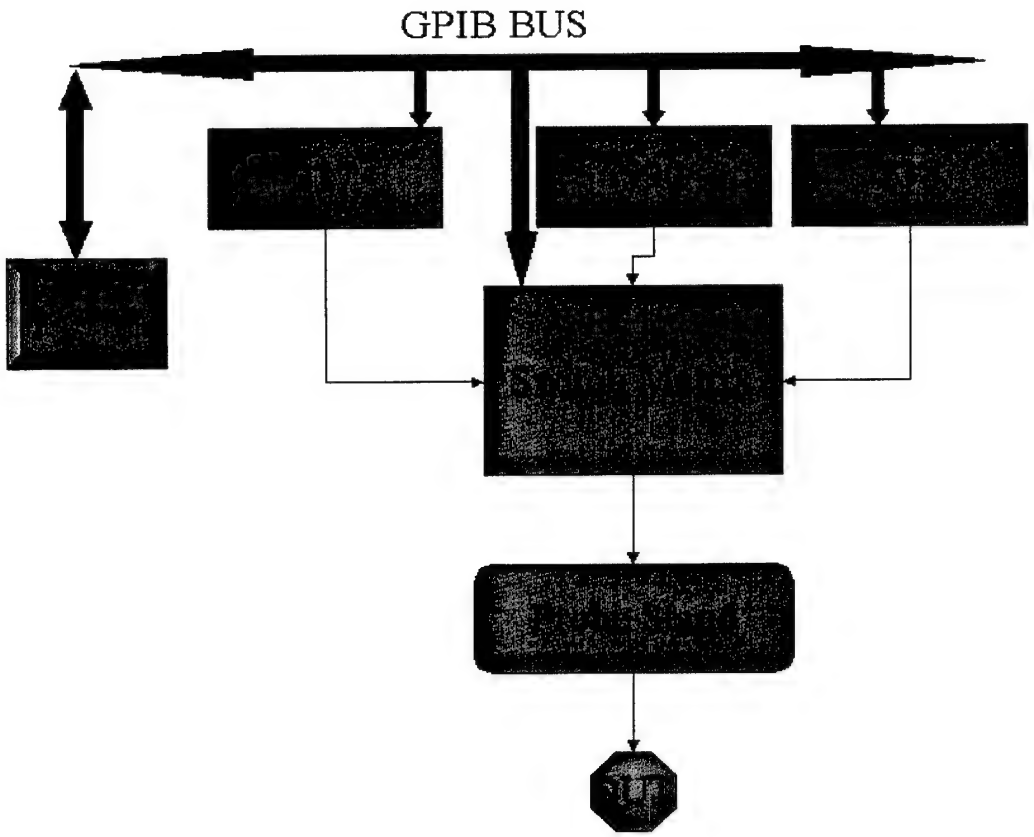

Figure 3.5: VASTAC test system block diagram used to control the automated I-V measurement setup.

The wafer is loaded onto the Micromanipulator Chuck and each device on the wafer was tested by sweeping the voltage up to a magnitude of 1100V and recording the voltage when a preset compliance between 50μA-3mA is reached. When desired, the Keithley model 238 was employed for a quick check of the forward voltage drop by sweeping from 0-4V and recording the voltage at a 1A compliance level. Data from each sample was recorded in Metrics™ and plotted in Microsoft Excel as a wafer performance prediction tool. The purpose of the random sampling was to make early predictions on the performance of the devices on each wafer. A typical random sample test for a 35mm wafer takes 1 hour. Later, however, the random sample testing became obsolete for 35mm wafers due to improvements in the speed of the pass/fail testing. If needed, a detailed parameter extraction using the HP 4156B could be performed, but was usually outside of the scope of the bulk random sampling. The parameter analyzer uses a more accurate approach to measuring the current-voltage characteristics than can be extracted by the Keithley 237 or 238, which are only accurate down to 100mV. These Keithley instruments actually measure the characteristics back at the SMU, but the parameter analyzer has a local measuring system that is implemented with a four probe setup. The first set of probes act as the source, and the second set act as the measurement. For the Keithley instruments, there is only one set of probes. In using the HP 4156B, the accurate extraction of parameters such as reverse saturation current (I_0), barrier height (Φ_B), and ideality factor (n) can be performed.

Also beyond the scope of the random sampling testing were capacitance-voltage measurements, which could be performed on a Keithley model 590. The 590, which is

also controlled with Metrics ICS, was occasionally used to sweep the devices from 0V to –20V to determine the effective doping density (N_D-N_A), to provide a comparison of the accuracy of the current-voltage measurement of the barrier height, to give an accurate extraction of the built-in voltage (V_{bi}), and to give the zero bias capacitance (C_0). However, as previously stated, these measurements were not made on all devices in the interest of time.

Automated Pass/Fail Testing Methodology

The automated testing system was implemented using the switch matrix, the Keithley models 237 and 238, and the semi-automated capabilities of the Wentworth Labs probe stand. All of the equipment employed was controlled using National Instruments' control software LabVIEW™ 5.0. The wafer was loaded onto the hot chuck. The actual test consisted of either forcing a current and measuring a voltage or applying a voltage and measuring the resulting current. In the interest of time, only a point measurement was taken rather than performing a full sweep. Four of these point measurements and the pass/fail parameters were defined by the user in LabVIEW™. Real-time measurements are reported back to the user as well as an auto-generated pass/fail wafer map. Upon completion of the 800-1500 devices tested, up to five output files are generated. The first output file contains the pass/fail data which becomes the input file for the die inking process that concludes the testing procedure. The other output files contains the current or voltage values for up to four points tested. This data is used to correlate device performance as a function of location on the wafer. The data is

analyzed in Microsoft Excel ™ and can easily be mapped and compared to early epilayer thickness or Capacitance-Voltage profiles for statistical data analysis purposes.

All data for each and every wafer and device is stored in a Microsoft Access ™ database [26]. The database provides a very quick method for examining the results of a wafer's characteristics, tracking the location of the wafer, and keeping track of the fabrication processes. The database currently contains records on 84 different wafers.

CHAPTER IV

EXPERIMENTAL RESULTS

In this chapter the results from the random sample testing and the pass/fail testing from Chapter Four will be presented. Also, the characterization and statistical data of the SBD's is discussed. The forward bias characterization and reverse bias characterization will be given following the presentation of the results from the random sampling test. Then, following the pass/fail results, the yield data will be presented as a comparison to predicted data in the random sample tests. The goal of this chapter is to report the results as they were found. Chapter Five will provide an analysis of these results.

Random Sample Testing

In random sample testing, the user records the reverse breakdown voltage and forward voltage drop of each of the 52 samples on the wafer using the preset current compliance levels. With this method, it was easy to make quick predictions on the performance of the wafer Figure 4.1 shows the random sample results from one of the wafers. This data was collected and organized into histograms as shown in figure 4.2. This particular wafer had a predicted yield of 53.8% with an average breakdown voltage of 178V for the argon implanted JTE and 147 V for the field-plate overlap JTE. The forward bias voltage drop for the devices was typically greater than 2.5V at 1A for the pre-packaged Ar-implanted JTE and the field-plate overlap JTE devices, respectively.

Wafer Number	AC0437-10		Date	12/27/00	Compliant	500uA	
Population	400		Population	400			
Random Sample Size	52		Random Sample Size	52			
Device Type	Ion Implan		Device Type	Field Plate		400um Devices I	
Sample	RBDV		Sample	RBDV		Sample	RBDV
1	100	sb	1	70		1	75
2	260		2	0		2	40
3	0		3	0		3	20
4	0		4	170		4	30
5	0		5	130		5	20
6	155		6	150		6	90
7	160		7	180	sb	7	200
8	50		8	110		8	350
9	60		9	40		9	350
10	160		10	110	sb	10	220
11	60		11	180		11	220
12	0		12	0		12	230
13	45		13	190		13	310
14	0		14	150		14	175
15	190		15	190		15	275
16	230		16	40		16	220
17	0		17	130		17	200
18	160		18	80		18	40
19	0		19	150		19	0
20	120	sb	20	60		20	250
21	0		21	150		21	130
22	0		22	60		22	320
23	100	sb	23	110	sb	23	45
24	150		24	120		24	260
25	0		25	145		25	275
26	0		26	170		26	275
27	80		27	160		27	70
28	60		28	180		28	230
29	0		29	150		29	130
30	120	sb	30	0		30	360
31	180		31	0		31	75
32	200		32	130		32	340
33	180		33	140		33	180 sb
34	0		34	80		34	350
35	130		35	80		35	40
36	190		36	60			
37	60		37	60			
38	175		38	40			
39	40		39	140			
40	40		40	120	sb		
41	40		41	275			
42	0		42	100			

Figure 4.1: Random sample sheet

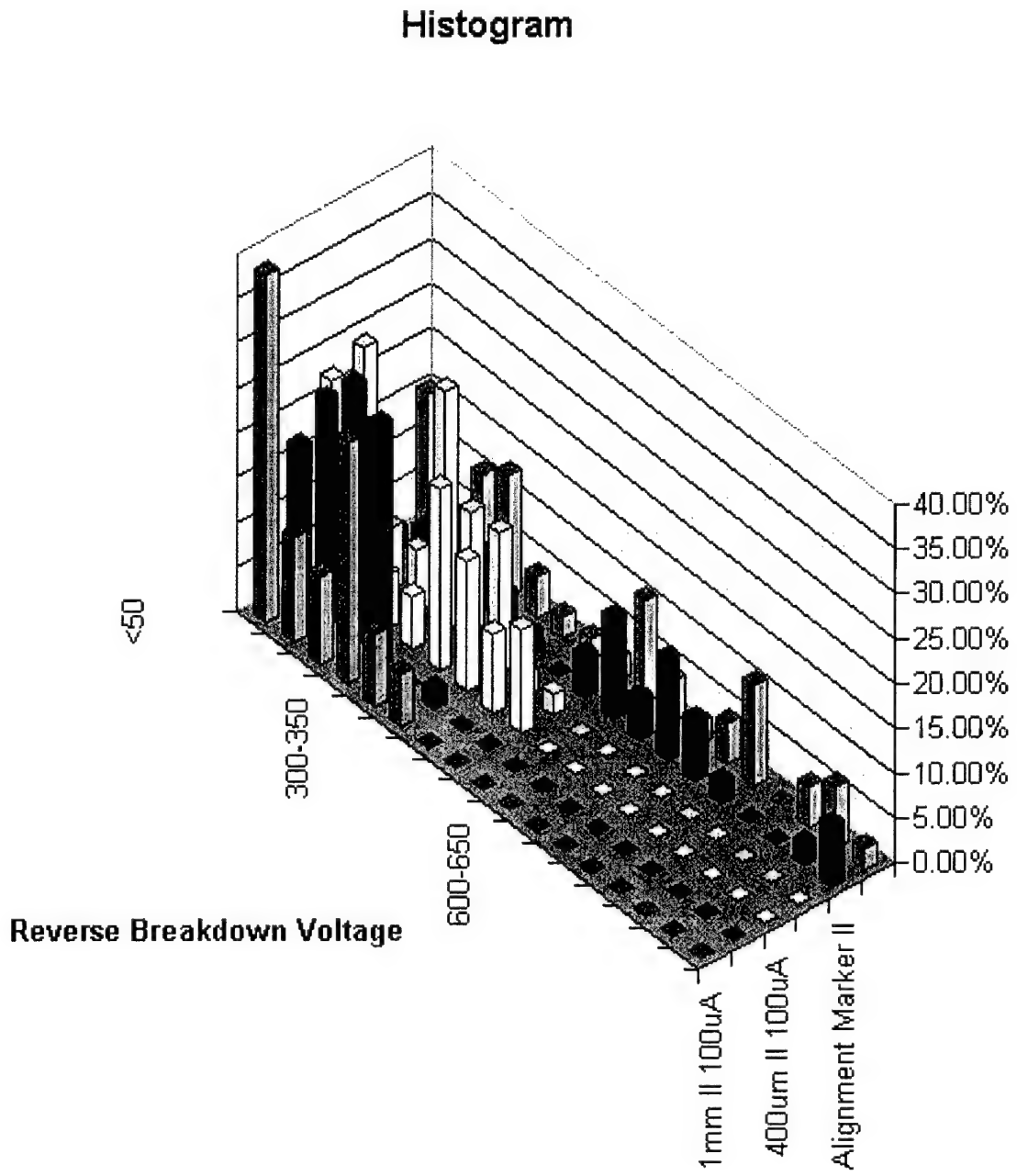

Figure 4.2: Histogram generated from random sampling of the reverse breakdown voltage vs. SBD edge termination style and anode contact size.

Forward Bias Characterization

The HP 4156B may be employed for more detailed forward bias characterization. This tool is useful in extracting data such as leakage or saturation current density (J_0), barrier height (Φ_B), ideality factor (n) and on-state resistance (R_{on}). The log current-voltage curve shown in figure 4.3 is from a single field-plate device on wafer number U0377-03 at room temperature. This field plate SBD displays a leakage current of 861nA, a barrier height of 0.665 eV, and an ideality factor of 1.11. The method for extracting the above characteristics is relatively simple using the parameter analyzer. By plotting the current on a log scale the regimes of operation can be seen. By extrapolating the first linear regime of the log (I) versus V_A to the y-intercept, a value for the saturation current can be extracted [21]. The typical value for the saturation current was approximately 800 nA or 0.086mA/cm^2 . By rearranging equation 2.17, the barrier height is found to be

$$\Phi_B = \frac{kT}{q}\ln(\frac{A^*T^2}{J_0}) \tag{4.1}$$

The typical value for the barrier height calculated from equation 4.1 is 0.65-0.85 eV. Next, the ideality factor, n, can be extracted by manipulating the current equation 2.19 into a logarithmic slope-intercept form to get the following:

$$\ln(J) = \frac{q}{nkT}V_A + \ln(J_0) \tag{4.2}$$

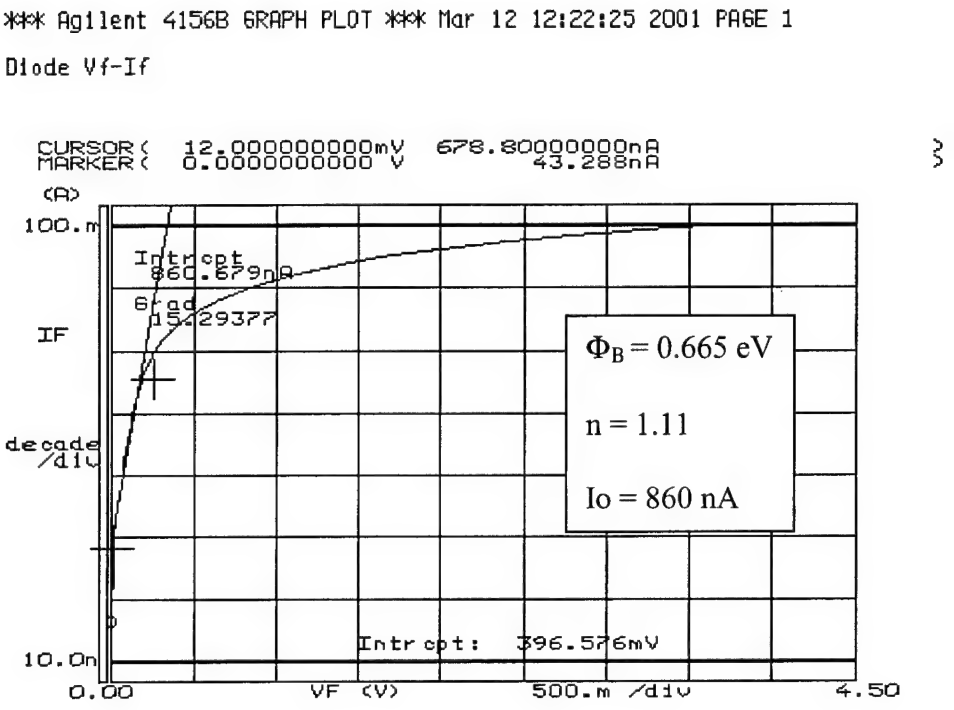

Figure 4.3: Forward bias performance of an unpackaged device from wafer U0377-03: Log (I) vs. V_A.

By finding the slope of the same linear portion mentioned earlier, the ideality factor may be extracted from the curve. Typically, it was found to be around 1.1-1.25 for these unpackaged diodes. Typically software tools such as metrics and most other pieces of equipment plot the current on a base 10, logarithm scale rather than a natural logarithm scale [21]. This requires an additional small change to the above equation, which is required when data extracting from most laboratory tools:

$$\mathbf{n} = \frac{q}{\ln(10^{m})kT} = \frac{q}{2.3mkT} \tag{4.3}$$

where m is the slope of the linear portion, or recombination, regime. It should be noted that Microsemi Inc. later packaged the diodes. Upon packaging the diodes, the value of the barrier height and ideality factor remained within the pre-packaged range. Figure 4.4 shows data from one of the actual devices packaged by MicroSemi. This device, which was taken from wafer CV0036-10, clearly shows a lower saturation current, but it possesses a barrier height on the upper end of the scale at 0.85 eV. The ideality factor is 1.25.

Finally, the series resistance can be extracted from the high-level injection (HLI) regime that is the final linear portion of the forward-bias I-V curve [21]. The extraction is accomplished by using the following equation on data in the HLI operating regime:

$$R_{on} = \frac{\Delta V_A}{J} \tag{4.4}$$

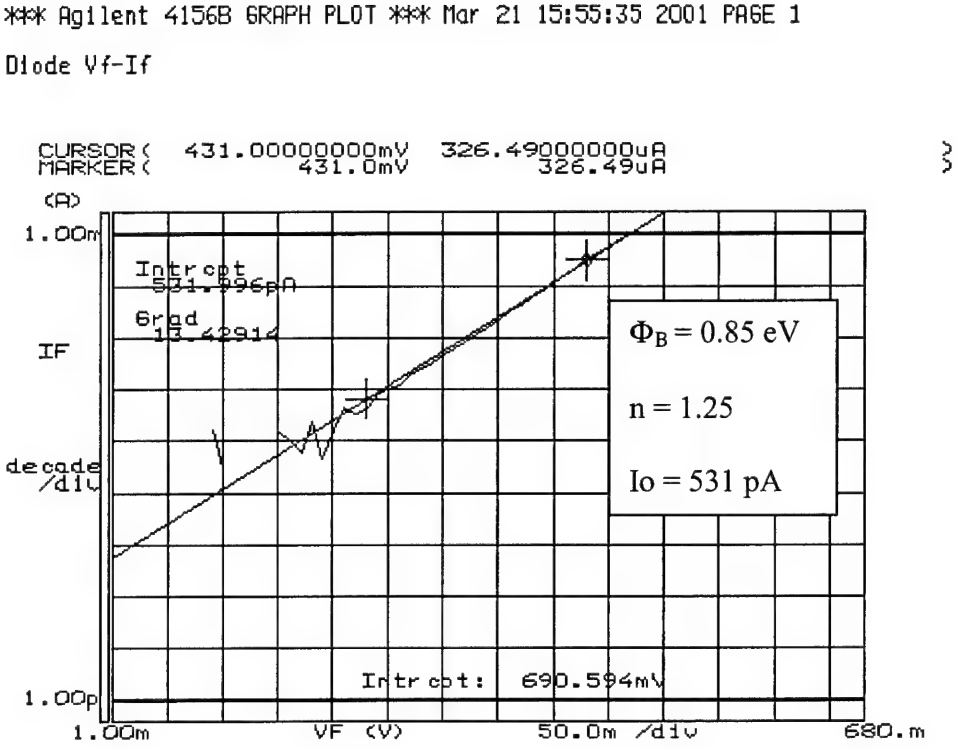

Figure 4.4: Packaged device from wafer CV0036-10: Log (I) vs. V_A

The typical series resistance was 300mΩ/cm^2 for the implanted devices and field-plate devices. However, upon packaging the devices, the diodes performed much better by displaying a lower on-state resistance. In forward bias, the field-plate overlap devices consistently performed identically to the implanted devices.

Reverse Bias Characterization

Reverse bias characterization is relatively simple compared to that of forward bias characterization. An extrapolation of the log-current to intercept the y-axis gives the reverse bias saturation leakage current (which ideally should match that of the forward bias extrapolation). Extrapolating the current-voltage curve in the avalanche regime to the x-axis intercept gives the breakdown voltage. Otherwise, the user selects a voltage and basically reads off the leakage current at that voltage. Crofton and Sriram have performed investigations on exactly what type of reverse leakage currents were active under an applied reverse bias [2]. Upon consulting with Dr. Crofton directly, simulations were performed using his software with the design parameters and the extracted characteristics of the MCASP SBD's [28]. It was found that the SBD's did not follow the thermionic emission or field emission models, but did closely follow to the thermionic field emission model. The model and the actual device reverse bias characteristics are shown in Chapter Five. The field-plate overlap devices typically held off 35% less voltage that the Ar-implants, and the leakage was typically 50% less in magnitude prior to breakdown. The final wafer values shown in Appendix B were taken at a compliance of 1mA. At reverse currents greater than 1mA, catastrophic failures

would occasionally occur at various places on the device, rather than directly under the probe tip. The failures burned through the device from the needle to the hot-chuck.

Pass/Fail Testing and Yield Analysis

Pass/fail testing is performed for two main purposes: providing yield information and mapping the wafer according to performance. The yield information is important for processing wafers so that corrections may be made to improve production and to make sure that no bad devices are packaged and sent to customers. The wafer map helps out in the production side by correlating the performance of devices to epilayer thickness profiles, doping profiles, etc. The pass/fail test was performed on each wafer. The pass/fail results from 50mm wafer AE659-06 are shown in figure 4.5. The final results from these acceptance tests for every wafer can also be found in Appendix B. This table contains the test conditions that were selected to determine whether or not the device was accepted and the percent yield of each wafer. Also in the table is the important figure of predicted yield that was gathered from the random sample testing. Due to a change in the customer requirements for the SBD's, only a single reverse bias point was taken at 1mA to reduce testing time consumed in the testing. A typical pass/fail test could take anywhere between 1.5 – 4 hours depending on the wafer size and the condition of the wafer. Following the pass/fail testing of the first six wafers, two wafers were inked and shipped to the customer. Although the yield of the wafers was not always high, the actual yield was always within 10% of the predicted yield if tested under similar conditions. The factors affecting the poor yield are discussed in the next chapter.

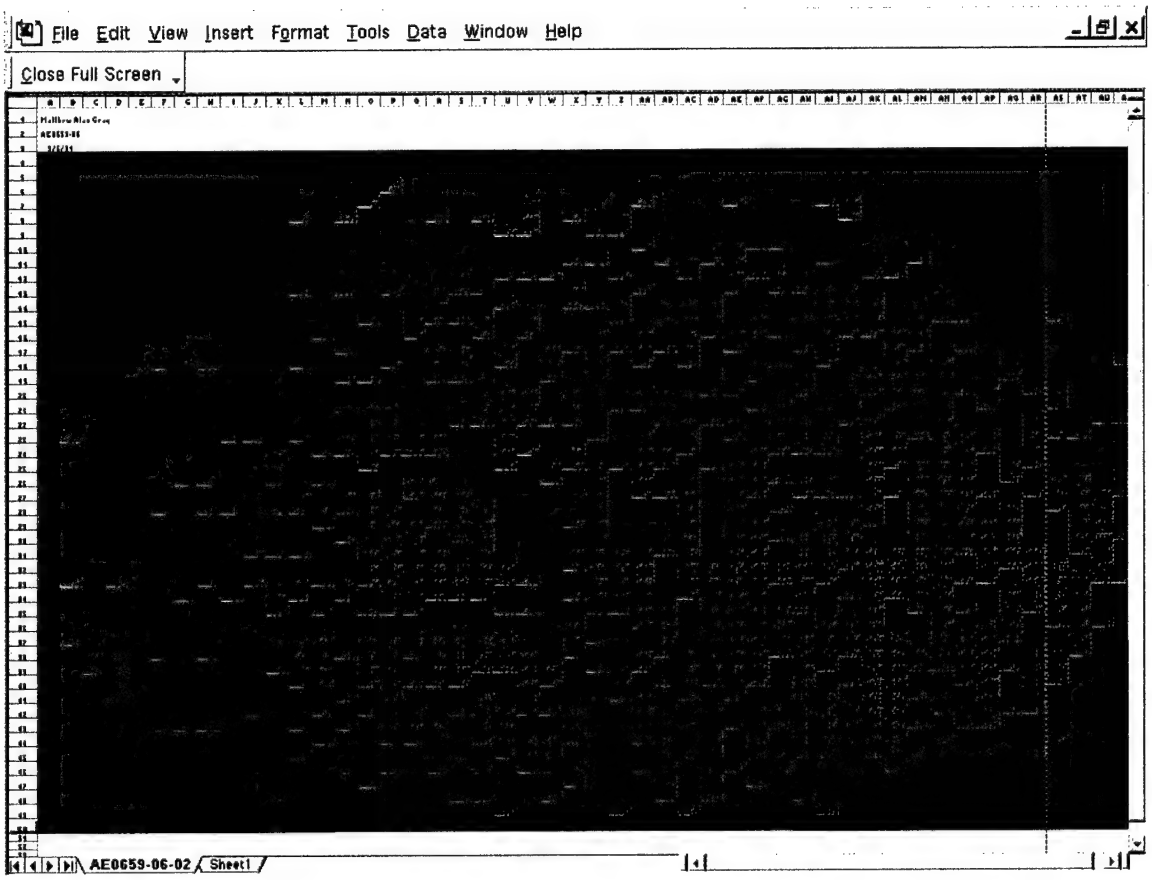

Figure 4.5: Pass/Fail wafer map of wafer AE659-06 : Pass >= 100V = Green, Fail < 100V = Red.

CHAPTER V

DISCUSSION OF RESULTS

This chapter presents a discussion of the results that were obtained in this work. Presented first are the issues associated with the two different types of edge terminations and their effects on device performance. Next, the investigations into area scaling are discussed followed by conclusions on the influence of the SiC substrate are offered. Finally, to conclude this work, recommendations are offered for a more optimal device based on lessons learned.

Edge Termination Issues

Wafer AB0348-01 displayed significant differences in the performance between the argon implanted devices and the field-plate overlap devices. Figure 5.1 shows the difference for the two devices under reverse bias. The argon implants showed a much higher hold-off voltage in reverse bias than that of the field plate. However, the argon terminations displayed very high leakage currents before moving into avalanche.

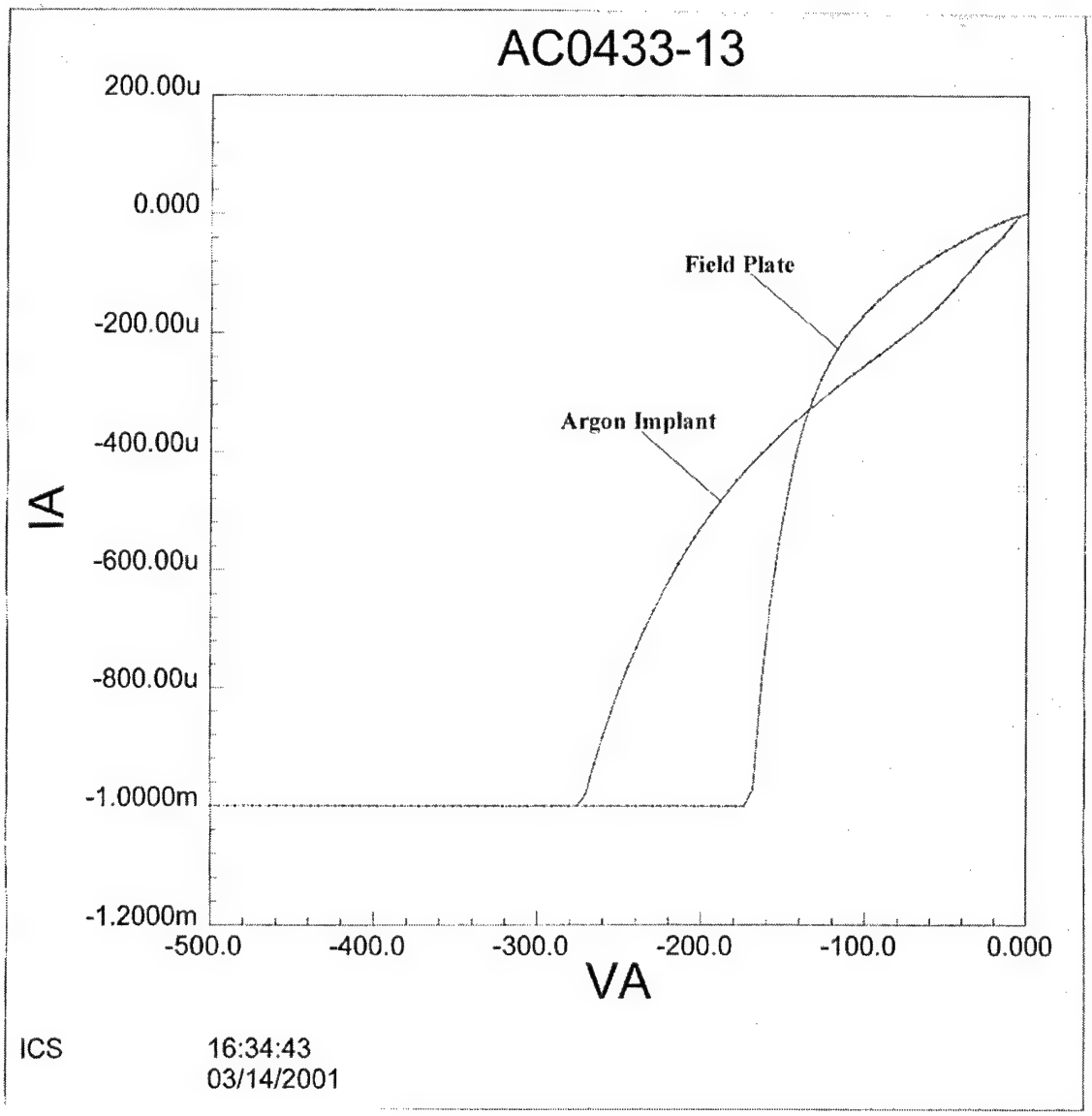

Figure 5.1: Typical reverse bias performance from wafer AC0433-13 comparing argon implant terminated SBD's to field plate terminated SBD's.

The field plate devices displayed very low leakage compared to the implanted devices and although they did not have as high of a breakdown voltage, they consistently displayed breakdown within 50 volts of preceding devices on the wafer and immediately snapped into avalanche conduction. The typical standard deviation of the field plate devices was ± 40V whereas the standard deviation for the implanted devices was over a factor of two greater at ± 88V. Figure 5.2 shows the mean value and standard deviation for the two types of devices on each wafer. This graphic clearly shows the difference in performance between the two devices.

Another interesting correlation comes from the comparison between figures 5.2 and 4.4. The 50mm wafer, AE659-06, shows very little variance between the two types of terminations that is clearly defined between the two graphics. This makes it difficult to distinguish between the two types of devices. However, in observing a wafer such as AB0402-07 in figures 5.3 and 5.4, the difference is obvious between the two regions. In figure 5.3, the devices displaying breakdown greater than 300V were shown in green, and the devices between 200 and 300 volts were shown in red. It is easily observed that the field plate terminated SBD's are in the lower half of the wafer and the argon implanted devices are in the upper half. Figure 5.4 is a surface/voltage plot that clearly separates the erratic argon implanted region from the smoother field-plate region.

For consistency and low leakage, the obvious choice is the field plate overlap devices. For higher reverse breakdown voltages in applications where leakage is not a significant factor, the argon implanted rectifiers are the devices of choice.

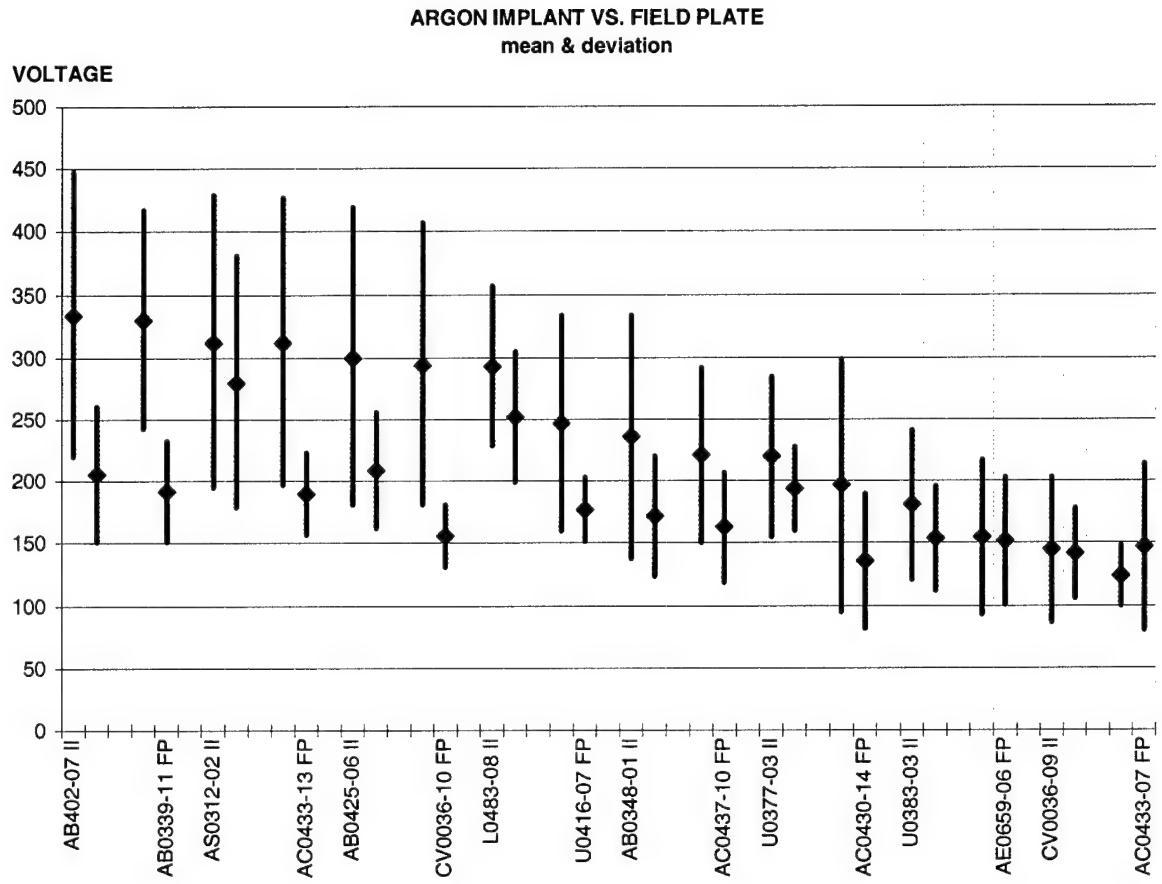

Figure 5.2: Statistical comparisons of argon implant devices and field plate devices

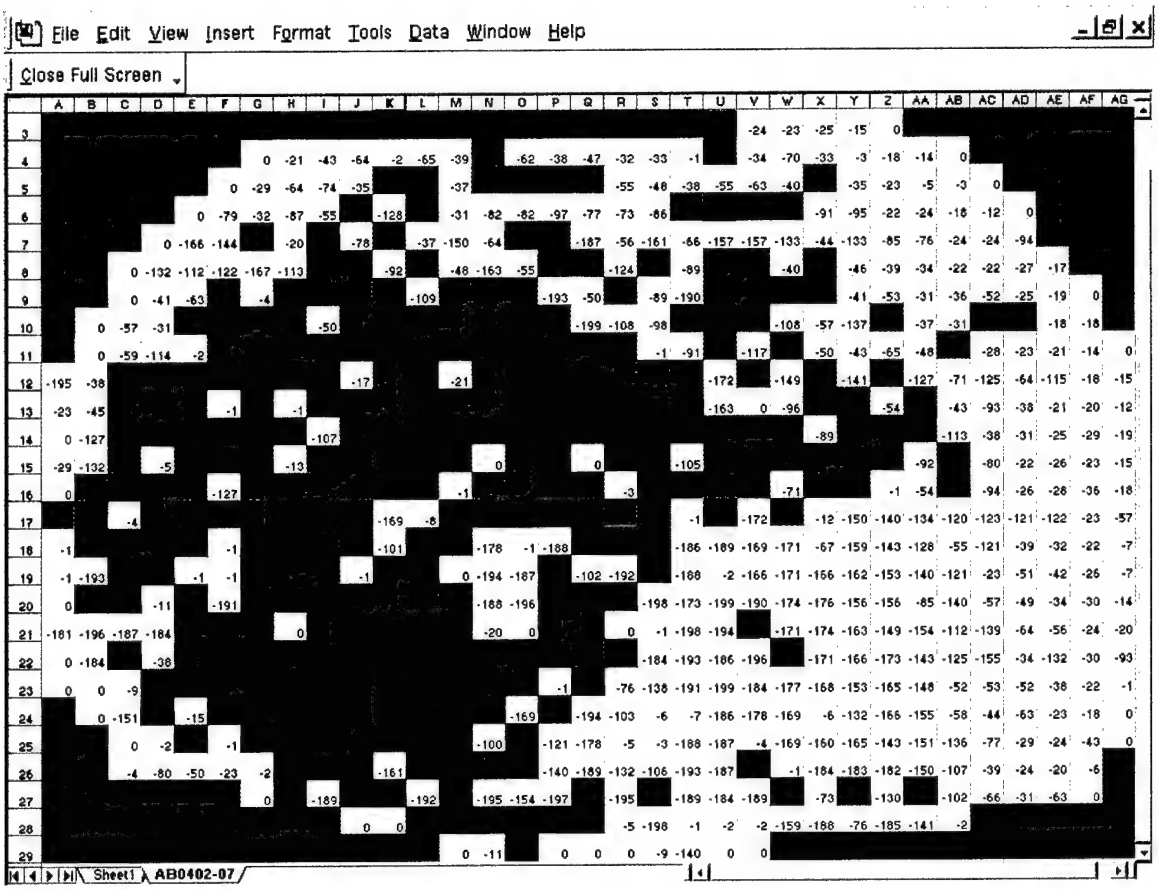

Figure 5.3: Wafer AB0402-07 Pass/Fail results and argon implant region vs. field plate region.

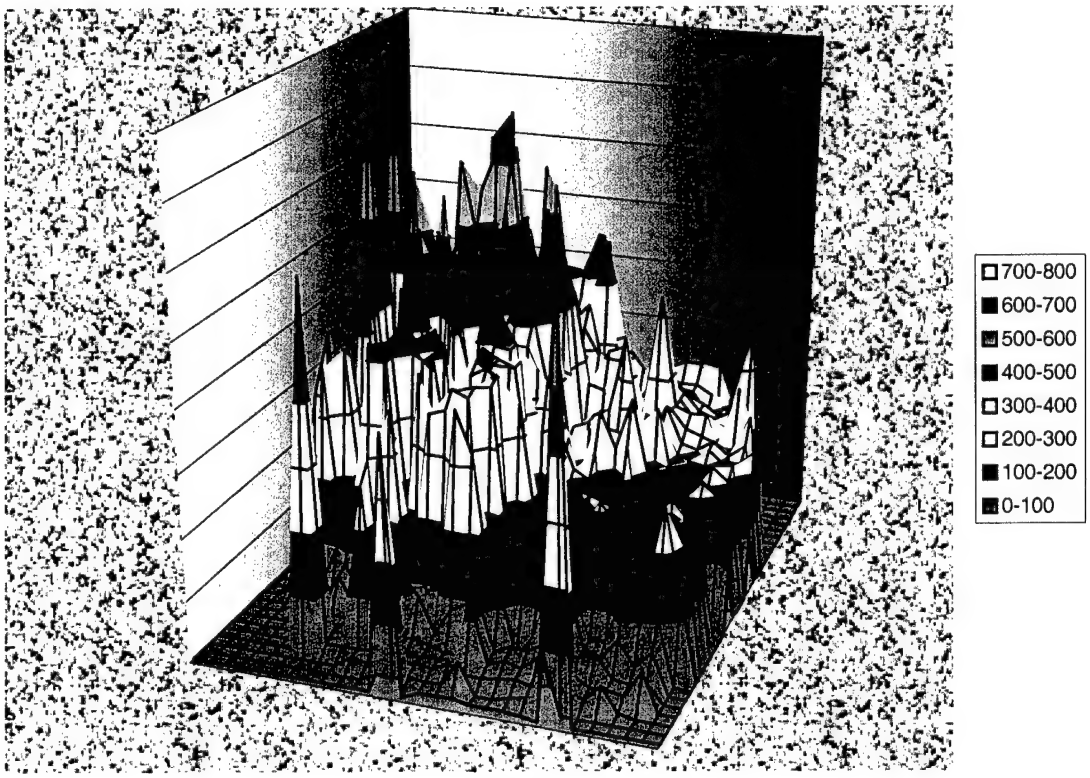

Figure 5.4: Wafer AB0402-07 surface voltage plot: argon implant region vs. field plate region.

The most likely source of the excess leakage current is surface leakage across the resistive implant layer. Baliga has shown that the high leakage current is directly related to the argon implant damage [29]. He demonstrated that the leakage in his devices are three orders of magnitude greater than his unterminated devices. It is estimated by simulations that the SBD's are only using up to 10 μm of the 30 μm of the resistive implant from the edge of the Schottky contact. This is due to the fact that the equipotential lines only extend 10 μm from the edge of the metal. In order to completely utilize the entire area of the implant, the dose of the implant must be increased. This would extend the equipotential lines to the edge of the implant thereby increasing the reverse breakdown voltage. Unfortunately, this also drastically increases the leakage currents across the surface. The reasons for initially considering the argon damage implants were that the implant is reliable in producing high voltage devices and is relatively easy to fabricate [29]. They are easy to fabricate because argon implants do not require annealing for activation, which is required for p-type implants. However, though this is a relatively easy termination compared to other implant termination strategies, it is more expensive.

MCASP is, however, fully capable of producing the much more reliable field plate terminated devices. The reason for the lower performance in the field plate terminated devices is attributed to the design precision that is required for manipulating the electric fields below the device [24]. Therefore some amount of design iteration is

required. Due to the low standard deviation of these devices, once the device design is perfected, the parametric yield should greatly improve.

The most likely explanation for the devices investigated not following the ideal thermionic emission model is that the model does not take into account any quantum mechanical tunneling through the Schottky barrier [2]. Due to the very high electric fields that are possible in 4H-SiC, tunneling is the predominant factor in reverse leakage currents. This introduces several orders of magnitude of error in a basic thermionic emission model which could be helped by changing the Richardson's constant [30]. Upon discussing this with Dr. Crofton [28], his software was used to create arguably the most important product of this work.

Figure 5.5 shows another comparison between the log currents of an argon implanted device, a field plate device and a thermionic field emission model produced from Dr. Crofton's software. Clearly the argon implant does not follow any theoretical model. It is most likely overwhelmed with anomalous surface leakage across the resistive implant. However, the field plate terminated device follows almost identically to the thermionic field emission model presented by Crofton [2] for approximately one-third of the overall breakdown voltage. The model was fit to the raw data using a barrier height of 0.707 eV, which was well within the previously measured range of 0.65-0.85 eV. The doping density used for the model was 5×10^{15} cm^{-3} as prescribed in the design. Finally, the temperature at which this data was taken was 294 K. These results correspond exactly to what was predicted from the literature as stated in Chapter Two.

At the point where Crofton's model shifts to the field emission model, the MCASP field plate diode begins to exhibit anomalous leakage current most likely from material defects. It is also reported that the thermionic emission model was four orders of magnitude lower than the actual data.

Substrate Defect Issues

Upon searching for the cause in the discrepancy in the calculated and measured breakdown voltages the issue of material defects came into question. Figure 5.6 shows a close-up of the surface of a wafer following epilayer growth, but prior to any other fabrication procedure. When compared to investigations performed by Neudeck and others in figure 5.7, it may be concluded that elementary screw dislocations and micropipes may have played a role in increasing the leakage current thereby lowering the reverse breakdown voltage [31, 32]. What resembles growth pits, elementary screw dislocations, and micropipes are evident on the surface of the device as shown through the metal. This immediately suggests that a larger size device will be infected with more defects if the defect concentration is too great.

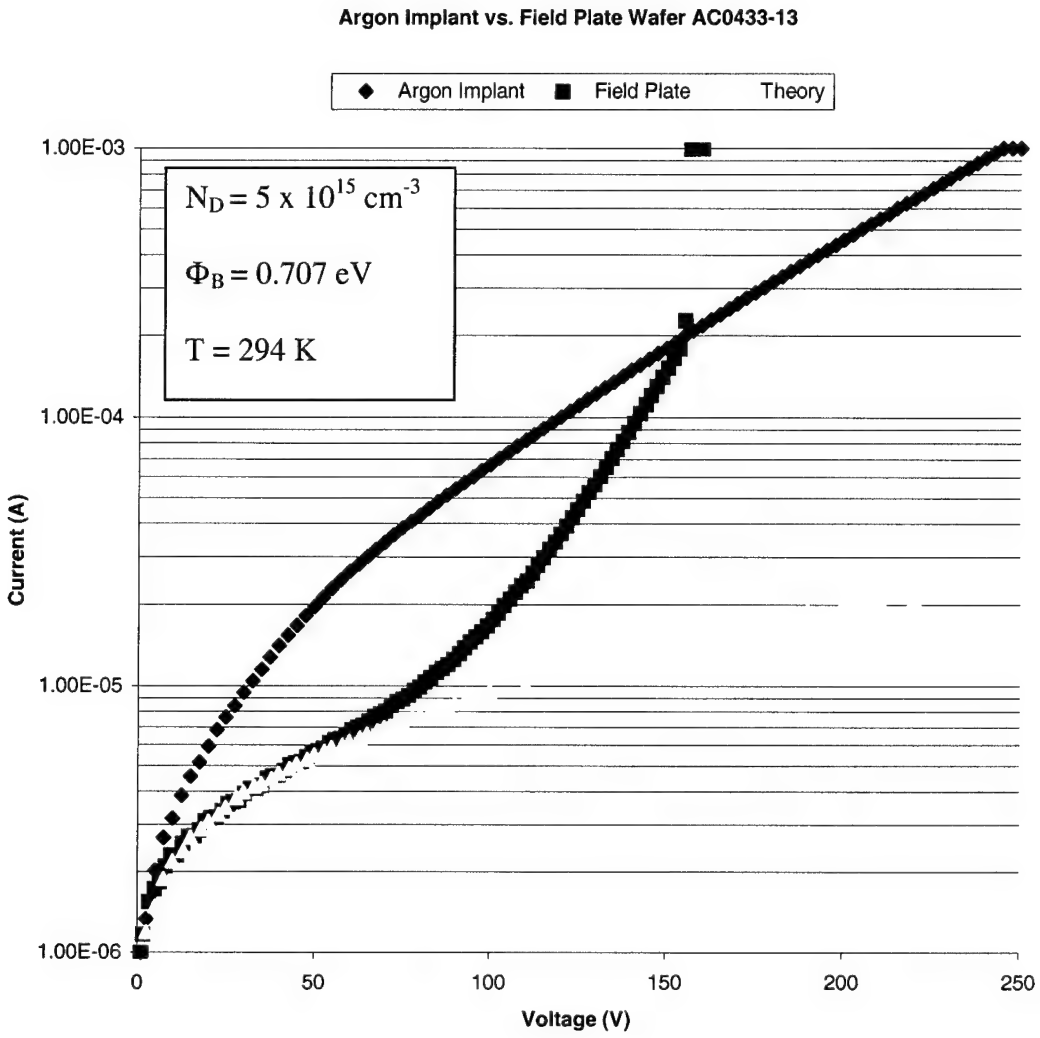

Figure 5.5 Thermionic field emission simulation vs. raw data from argon implant and field plate devices.

Area Scaling Issues

As mentioned earlier, an optimal device size must be established for optimal performance in these devices. In these investigations, it is easy to conclude that the larger devices perform much better in forward bias, and the smaller devices hold off more voltage. The current-voltage plots in figure 5.8 show the three device sizes and their corresponding performance. Clearly in this figure, the 100μm alignment markers hold off more voltage, but the small device cannot handle the 1mA of current that the two larger devices can. Virtually all of these devices had catastrophic failures when they went into avalanche breakdown. The 400μm devices consistently withstood more voltage than the 1mm contacts, but did not measure up in its forward bias conduction capabilities. However, it is difficult to draw conclusions on this matter due to the fact that none of these smaller devices were packaged. It is possible that these devices would perform just as well as the devices from the previous investigations section due to the resulting decrease in series resistance from the Microsemi packaging. Figure 5.9 shows the wafer-level forward bias comparison of the three sizes of devices.

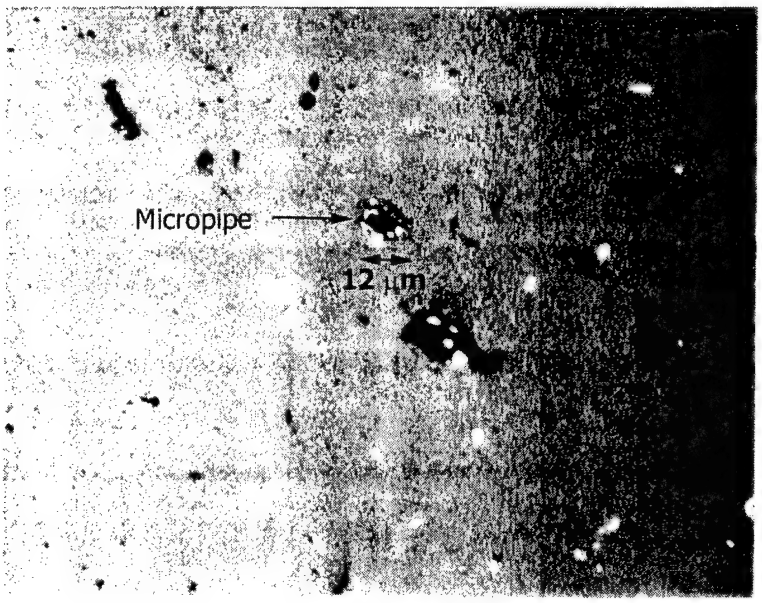

Figure 5.6: Surface close-up of a wafer following epilayer growth in EMRL.

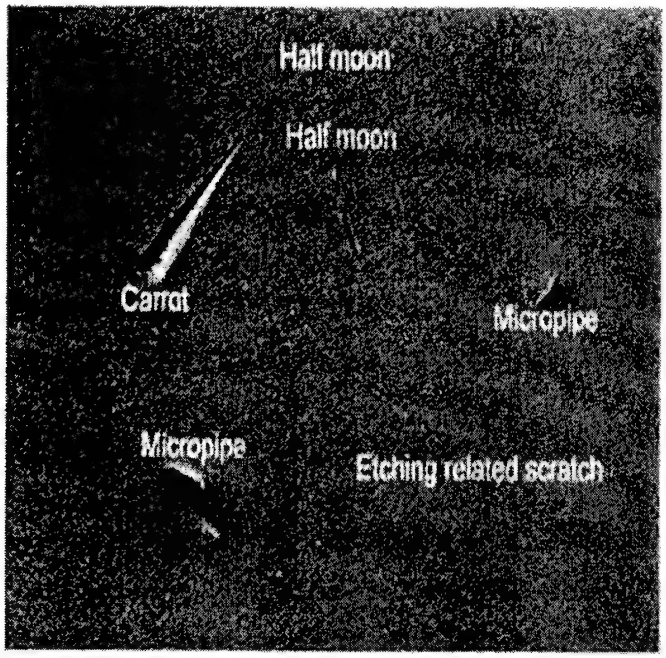

Figure 5.7: Surface close-up of SiC substrate after epitaxial growth (from [31])

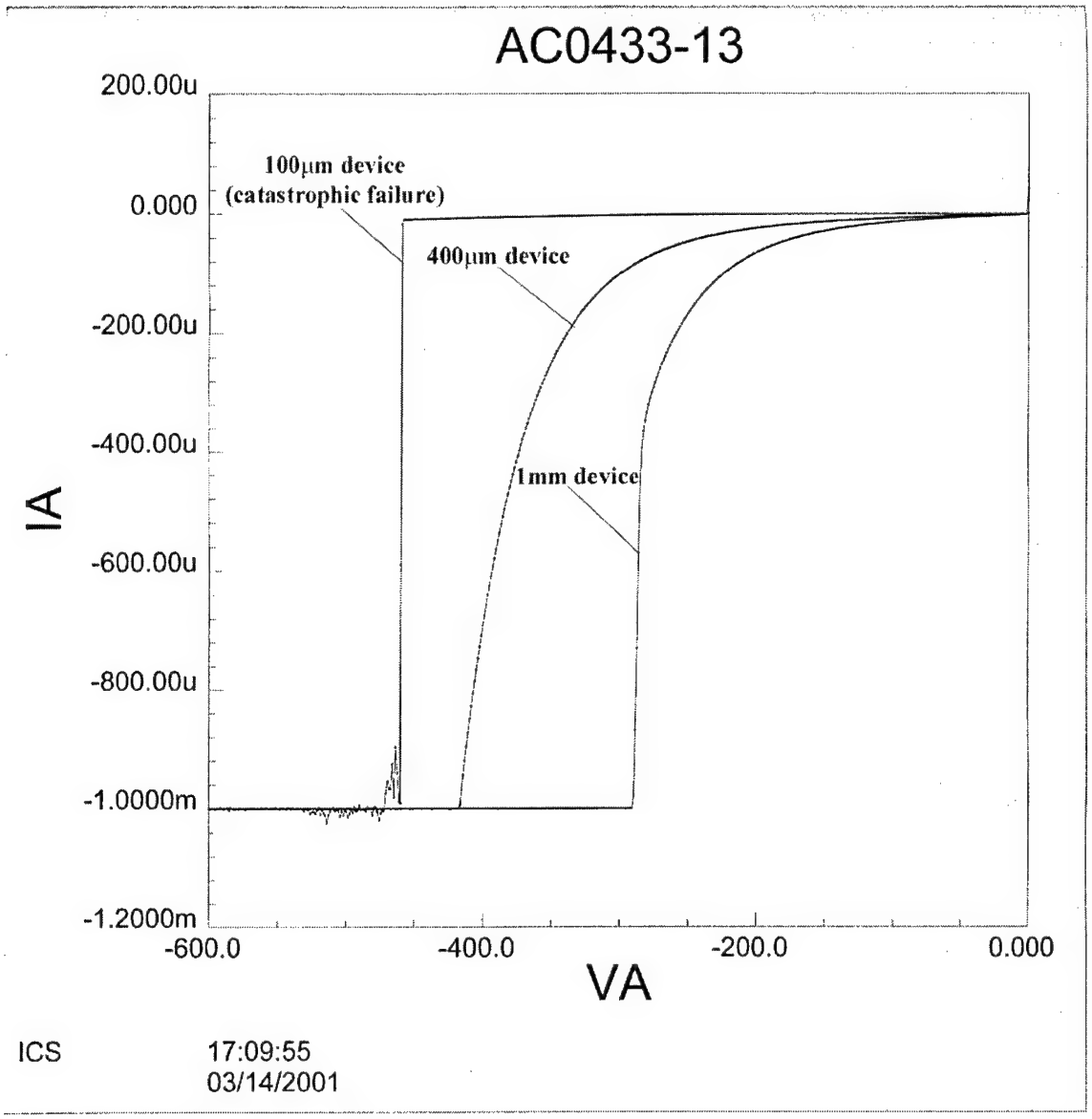

Figure 5.8: Reverse bias comparison between 1mm, 400 μm, and 100 μm SBD's from wafer AC0433-13

Insight for Device Improvement

Although these devices did not meet their 600V design goals, they are successfully manufactured SiC Schottky barrier diodes. In order to improve the performance of these devices several changes need to be made, the first of which begins with the substrate. The Cree SiC substrates that were used in the fabrication of the SBD's were both research grade and "non-sorted" grade. Appendix A shows all of the data and characteristics associated with the Cree wafers. Appendix B relates the grades of the wafers to the yield produced from each of the wafers used. It is believed that although the doping of the substrate is accurate, the physical defects of the wafers were too abundant to accomplish the 600V to 800V design goals. Therefore, it is recommended that the next lot of SBD's be fabricated using at least a production grade wafer. Next, by using p-type implants rather than a neutral argon implant, the leakage in the SBD's may reach acceptable levels. Boron and aluminum implants are commonly used in the place of argon [5, 11, 12]. A promising alternative to exploring a new type of edge termination is working on perfecting the electric field manipulation with the field plate terminations. This will involve a very tedious design process, but the end result would drastically improve yield. Next, the epilayer doping was correct, but the thickness was slightly less than what was desired, thereby immediately decreasing the breakdown voltage as demonstrated in equation 2.22. Figure 5.3 actually shows what is suspected to be a "wedge" of epi, which extends from the lower right corner to the upper left corner. By finding an optimal size device, the wafer area can be fully utilized to produce the

maximum amount of devices. Finally, another improvement to the SBD's could be to increase the metal work function by selecting another metal other than titanium. It is well known that in SiC the barrier height is strongly dependant on the difference between the metal work function and the electron affinity of SiC. Therefore metals with lower work functions such as Ti, Al, W, and Cr may form good ohmic contacts and metals such as Pt, Ni, Pd, and Au may form good Schottky contacts [33]. Some of metals with intermediate work functions are able to form both types of contacts. The selection then becomes a matter of metal adhesion.

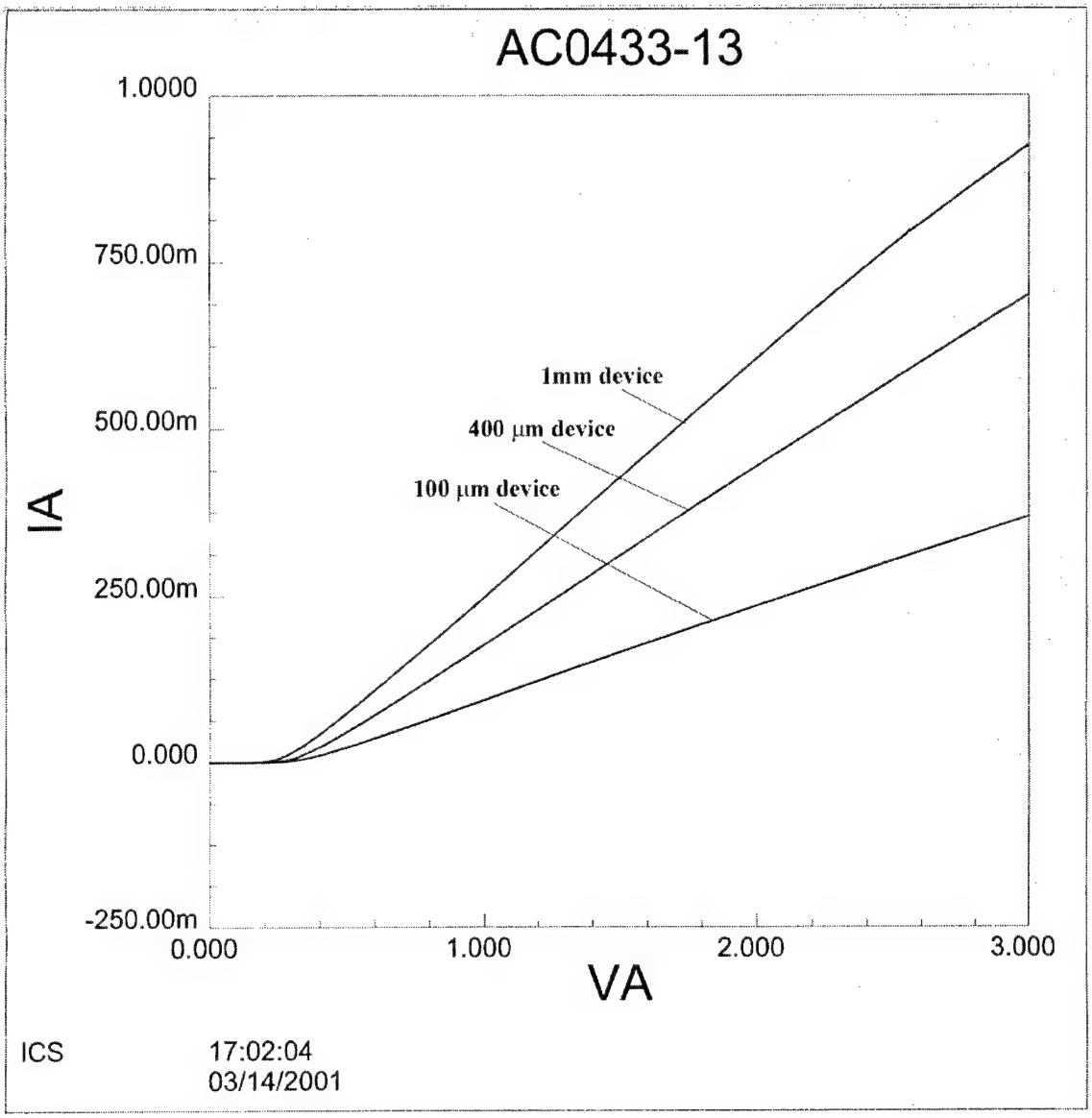

Figure 5.9: Forward bias comparison between 1mm, 400 µm, and 100 µm SBD's from wafer AC0433-13.

CHAPTER VI

CONCLUSIONS

This thesis contains a collection of data from 18 wafers and over 15,000 4H-SiC Schottky barrier diodes. Statistical yield analysis has been presented in a manner that can help improve future production efforts of such high performance rectifiers. Wafer-level statistical analysis was able to successfully predict the performance of each of the 18 wafers' lots investigated in this study.

The discussion of Chapter Two's theory of operation of the SBD was eventually tied directly to actual device performance. A correlation between the significance of the selection of the Schottky contact metal and the resulting barrier height of the device was demonstrated. For example, review of previous investigations led conclusions to be drawn that the selection of a metal with a higher work function would give a lower reverse leakage current which would allow for the rectifier to approach a more ideal model. A thinner epilayer compared to many of the previous investigations resulted in a slightly lower breakdown than desired. The types of terminations selected for the SBD's performed consistently with what has already been suggested in the previous investigations and with what theory and simulations predict of them.

Characterization of these rectifiers which shows the similarities and differences of argon implanted devices versus field plate overlap devices in both forward bias and reverse bias is provided in this work. The fact that the field plate terminated devices performed consistently at lower reverse bias voltages with a low wafer-level standard deviation was shown. In addition, the argon implants showed a higher breakdown voltage with a higher wafer-level standard deviation.

Characterization techniques and equipment used in this work was verified by comparing the data extracted in this work to data produced by Microsemi on the same devices. All data was closely associated with the exception of the on-state resistance, which was lowered as a result of the device packaging performed by Microsemi, as expected.

Also given in this thesis is a comparison of three different device sizes with 1mm contacts, 400 μm devices and 100 μm devices, respectively, which provides further insight to future development of the SBD's by helping find an optimal device size. It was clearly demonstrated that the smaller devices exhibited higher breakdown voltages in reverse bias, but produced poor forward characteristics.

This thesis has strongly tied a theoretical model provided by Crofton [2] to a typical device in the field plate terminated 4H-SiC SBD. The device's raw data followed the "ideal" model for a third of the overall breakdown voltage. When the argon implant terminated device was compared to the model, it became clear as to how far away from

ideal the devices were operating, and that they were dominated by anomalous leakage currents.

MCASP is currently investigating SiC SBD's and junction barrier Schottky diodes with various circular and square areas and with various edge terminations. The design of the new SBD's and advances toward optimal devices are a direct result of the exceptional MCASP engineering team and these investigations on the first lot of SiC Schottky barrier diodes fabricated at Mississippi State University.

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APPENDIX A

CREE SHIPPING FORMS

SiC Material Shipping Form

CREE

Customer: Mississippi State Unive
Ship Date: 26-May-00

Customer Order No: 990-25377
Part Number: W4NRD8C S000

Excel File Name: 5372
Sales Order No: 005372A

Item #	Wafer #	Resisitivity	Grd	Bare Substrate Thick. (us)	Diameter (inches)	Orientation	Manf. Date	Box ID	Semi-Spec	Other	MPD
Spec	NA	0.015 - 0.028	R	304.8 - 431.8	2.000"	8° +/- 30'	NA	NA	NA	NA	
1	AS0312-10	0.025	R	414.02µ	2.000	8°4'	000219	A	PASS		SEL
2	AE0659-06	0.015	R	414.02µ	2.000	7°54'	000430	A	PASS		SEL
3	AD0552-08	0.019	R	411.48µ	2.000	7°58'	000113	A	PASS		SEL
4	AS0337-03	0.023	R	403.86µ	2.000	7°59'	000417	A	PASS		SEL
5	AS0337-04	0.022	R	408.94µ	2.000	7°59'	000417	A	PASS		SEL
6	AD0552-05	0.020	R	398.78µ	2.000	7°58'	000113	A	PASS		SEL
7	AS0337-08	0.021	R	403.86µ	2.000	7°59'	000404	A	PASS		SEL
8	AS0312-05	0.026	R	408.94µ	2.000	8°4'	000210	A	PASS		SEL
9	Z0602-03	0.015	R	391.16µ	2.000	7°57'	000227	A	PASS		SEL
10	AD0589-08	0.016	R	396.24µ	2.000	8°6'	000415	A	PASS		SEL
11	Q0674-08	0.017	R	388.62µ	2.000	8°2'	000415	B	PASS		SEL
12	AE0637-11	0.016	R	403.86µ	2.000	7°57'	000404	B	PASS		SEL
13	AD0546-11	0.015	R	381µ	2.000	7°56'	000215	B	PASS		SEL
14	CV0036-11	0.016	R	421.64µ	2.000	8°2'	000217	B	PASS		SEL
15	AS0337-01	0.024	R	424.18µ	2.000	7°59'	000417	B	PASS		SEL
16	AS0312-09	0.025	R	429.26µ	2.000	8°4'	000210	B	PASS		SEL
17	AD0589-11	0.016	R	398.78µ	2.000	8°6'	000415	B	PASS		SEL
18	AD0589-10	0.016	R	411.48µ	2.000	8°6'	000415	B	PASS		SEL
19	CV0036-06	0.019	R	414.02µ	2.000	8°2'	000217	B	PASS		SEL
20	CV0036-02	0.021	R	424.18µ	2.000	8°2'	000217	B	PASS		SEL
21	AE0659-01	0.019	R	411.48µ	2.000	7°54'	000430	C	PASS		SEL
22	AE0619-08	0.022	R	414.02µ	2.000	7°55'	000210	C	PASS		SEL
23	CV0016-03	0.020	R	411.48µ	2.000	7°54'	000112	C	PASS		SEL
24	AD0547-05	0.019	R	391.16µ	2.000	7°59'	000110	C	PASS		SEL
25	CV0036-05	0.020	R	419.1µ	2.000	8°2'	000217	C	PASS		SEL
26	CV0036-03	0.021	R	419.1µ	2.000	8°2'	000217	C	PASS		SEL
27	AS0312-02	0.028	R	398.78µ	2.000	8°4'	000210	C	PASS		SEL
28	CV0036-10	0.017	R	403.86µ	2.000	8°2'	000227	C	PASS		SEL
29	AD0552-10	0.019	R	416.56µ	2.000	7°58'	000113	C	PASS		SEL
30	CV0036-09	0.017	R	426.72µ	2.000	8°2'	000217	C	PASS		SEL

CREE

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lssippi State University	26-May-00	990-25377	X4NXXXX	XXX0	5372

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1	AC0315-04	0.019	R	276.86	1.375"	7°38'	A-B	981001	YES
2	U0405-03	0.02	R	299.72	1.375"	8°6'	A-B	981022	YES
3	AC0329-07	0.018	R	261.62	1.375"	8°0'	A-B	980630	YES
4	U0292-09	0.018	R	368.3	1.375"	8°0'	A-B	971204	YES
5	L0480-04	0.02	R	297.18	1.375"	7°52'	A-B	990831	YES
6	AC0321-06	0.017	R	320.04	1.375"	7°55'	A-B	990831	YES
7	AB0339-11	0.017	R	322.58	1.375"	7°50'	A-B	990831	YES
8	AC0287-01	0.024	R	337.62	1.375"	8°0'	A-B	981202	YES
9	Z0426-07	0.018	R	299.72	1.375"	7°50'	A-B	990410	YES
10	U0291-04	0.02	R	330.2	1.375"	8°00'	A-B	971204	YES
11	AC0290-08	0.019	R	264.16	1.375"	8°00'	B-B	980220	YES
12	U0377-03	0.02	R	345.44	1.375"	7°54'	B-B	990831	YES
13	L0483-06	0.019	R	332.74	1.375"	7°58'	B-B	990831	YES
14	R0410-09	0.018	R	368.3	1.375"	8°06'	B-B	980923	YES
15	L0492-05	0.022	R	332.74	1.375"	8°05'	B-B	980925	YES
16	R0410-03	0.02	R	365.76	1.375"	8°06'	B-B	980923	YES
17	AC0433-07	0.018	R	312.42	1.375"	8°00'	B-B	990410	YES
18	U0418-11	0.017	R	294.64	1.375"	8°06'	B-B	981001	YES
19	Z0427-07	0.018	R	312.42	1.375"	8°00'	B-B	990410	YES
20	AB0348-01	0.021	R	325.12	1.375"	8°00'	B-B	990410	YES

stomer:	ShipDate	OrderNo	PartNumber	ExcelFileName	SalesOrderNoPlus
ssissippi State University	17-Aug-00	001-05727	X4NXXXX XXX0		005785B

CREE RESEARCH · INC

Item #	Wafer #	Resistivity	Grade	Thickness(μ)	Diameter	Orientation	Manf. Date	Box ID	MPD
1	AB0397-09	0.017	NS	322.58	1.375"	7°56'	981215	B	SEL
2	AE0436-02	0.018	NS	322.58	1.375"	7°46'	990226	B	SEL
3	AB0425-06	0.02	NS	403.86	1.375"	8°1'	990303	B	SEL
4	AC0430-14	0.018	NS	342.9	1.375"	7°56'	990319	B	SEL
5	AC0437-10	0.019	NS	332.74	1.375"	7°58'	990624	B	SEL

tomer:	ShipDate	OrderNo	PartNumber	ExcelFileName	SalesOrderNoPlus
ississippi State University	17-Aug-00	001-05727	X4NXXXX XXX0		005785D

CREE RESEARCH · INC

Item #	Wafer #	Resistivity	Grade	Thickness(μ)	Diameter	Orientation	Manf. Date	Box ID	MPD	D/S Polish
1	U0358-03	0.021	NS	276.86	1.375"	8°0'	981005	D	LMP	YES
2	AC0337-02	0.02	NS	276.86	1.375"	7°53'	981005	D	LMP	YES
3	U0387-06	0.019	NS	406.4	1.375"	7°46'	980930	D	LMP	YES
4	U0408-13	0.018	NS	299.72	1.375"	8°2'	981102	D	LMP	YES
5	AB0299-07	0.021	NS	236.22	1.375"	7°50'	981005	D	LMP	YES

stomer:	ShipDate	OrderNo	PartNumber	ExcelFileName	SalesOrderNoPlus
ssissippi State University	17-Aug-00	001-05727	X4NXXXX XXX0		005785C

CREE RESEARCH · INC

Item #	Wafer #	Resistivity	Grade	Thickness(μ)	Diameter	Orientation	Manf. Date	Box ID	MPD
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2	U0418-07	0.017	NS	284.48	1.375"	8°0'	980827	C	LMP
3	U0421-07	0.017	NS	284.48	1.375"	8°0'	981210	C	LMP
4	AB0402-07	0.016	NS	284.48	1.375"	7°54'	981112	C	LMP
5	U0416-07	0.017	NS	292.1	1.375"	8°0'	980829	C	LMP
6	R0405-04	0.02	NS	297.18	1.375"	7°58'	980901	C	LMP
7	U0401-04	0.02	NS	370.84	1.375"	8°02'	980727	C	LMP
8	AC0379-03	0.021	NS	317.5	1.375"	7°58'	980902	C	LMP
9	U0415-03	0.015	NS	314.96	1.375"	7°51'	980903	C	LMP
10	U0383-03	0.021	NS	276.86	1.375"	7°58'	980706	C	LMP

APPENDIX B

FINAL WAFER RESULTS

Argon Implaned

Wafer Number	Lot	Size	Grade	Predicted Reverse Breakdown Ave (all devices)	Predicted Typical Reverse Breakdown (good devices)	RS Compliance	%Predicted Yield >100V (Ar implant)
AE0659-06	1	50mm	R	51	108	30uA	23.6%
L0483-08	1	35mm	R	102	153	30uA	61.5%
L0492-05	1	35mm	R	94	189	50uA	50.0%
AC0433-07	1	35mm	R	10	N/A	30uA	0.0%
AB0348-01	1	35mm	R	***	***	***	***
U0377-03	1	35mm	R	117	134	50uA	81.6%
AB0339-11	2	35mm	R	79	171	100uA	37.6%
AC0430-14	2	35mm	NS	N/A	N/A	N/A	N/A
AE0436-02	2	35mm	NS	8	110	30uA	1.9%
AC0437-10	2	35mm	NS	101	178	50uA	50.0%
AB0425-06	2	35mm	NS	N/A	N/A	N/A	N/A
U0383-03	2	35mm	NS	N/A	N/A	N/A	N/A
AB0402-07	2	35mm	NS	84	170	100uA	38.5%
U0416-07	2	35mm	NS	N/A	N/A	N/A	N/A
AC0433-13	2	35mm	NS	N/A	N/A	N/A	N/A
AS0312-02	2	50mm	R	N/A	N/A	N/A	N/A
CV0036-10	2	50mm	R	N/A	N/A	N/A	N/A
CV0036-09	2	50mm	R	N/A	N/A	N/A	N/A

Field Plate Overlap

Wafer Number	Lot	Size	Grade	Predicted Reverse Breakdown Ave (all devices)	Predicted Typical Reverse Breakdown (good devices)	RS Compliance	Predicted Yield > 100V (Field Plate)
AE0659-06	1	50mm	R	49	N/A	30uA	0.0%
L0483-08	1	35mm	R	97	117	30uA	51.9%
L0492-05	1	35mm	R	63	129	50uA	26.0%
AC0433-07	1	35mm	R	2	N/A	30uA	0.0%
AB0348-01	1	35mm	R	***	***	***	***
U0377-03	1	35mm	R	148	189	30uA	71.4%
AB0339-11	2	35mm	R	67	112	100uA	28.4%
AC0430-14	2	35mm	NS	N/A	N/A	N/A	N/A
AE0436-02	2	35mm	NS	18	N/A	30uA	0.0%
AC0437-10	2	35mm	NS	105	147	50uA	57.7%
AB0425-06	2	35mm	NS	N/A	N/A	N/A	N/A
U0383-03	2	35mm	NS	N/A	N/A	N/A	N/A
AB0402-07	2	35mm	NS	139	192	100uA	65.2%
U0416-07	2	35mm	NS	N/A	N/A	N/A	N/A
AC0433-13	2	35mm	NS	N/A	N/A	N/A	N/A
AS0312-02	2	50mm	R	N/A	N/A	N/A	N/A
CV0036-10	2	50mm	R	N/A	N/A	N/A	N/A
CV0036-09	2	50mm	R	N/A	N/A	N/A	N/A

Wafer

Wafer Number	Lot	Size	Grade	RS Compliance	Predicted Wafer Yield >100V	Pass/Fail Compliance	Actual Wafer Yield >100V
AE0659-06	1	50mm	R	30uA	11.8%	50uA	7.7%
L0483-08	1	35mm	R	30uA	57.6%	50uA	86.4%
L0492-05	1	35mm	R	50uA	33.0%	50uA	24.8%
AC0433-07	1	35mm	R	30uA	0.0%	50uA	6.4%
AB0348-01	1	35mm	R	50uA	33.00%	50uA	27.7%
U0377-03	1	35mm	R	50uA	76.5%	50uA	81.8%
AB0339-11	2	35mm	R	100uA	33.0%	1mA	51.3%
AC0430-14	2	35mm	NS	N/A	N/A	1mA	6.0%
AE0436-02	2	35mm	NS	30uA	0.9%	N/A	N/A
AC0437-10	2	35mm	NS	50uA	53.8%	1mA	47.3%
AB0425-06	2	35mm	NS	N/A	N/A	1mA	70.0%
U0383-03	2	35mm	NS	N/A	N/A	1mA	39.9%
AB0402-07	2	35mm	NS	100uA	51.0%	1mA	61.0%
U0416-07	2	35mm	NS	N/A	N/A	1mA	58.8%
AC0433-13	2	35mm	NS	N/A	N/A	1mA	75.9%
AS0312-02	2	50mm	R	N/A	N/A	1mA	53.0%
CV0036-10	2	50mm	R	N/A	N/A	1mA	33.8%
CV0036-09	2	50mm	R	N/A	N/A	1mA	18.8%

APPENDIX C

MCASP FACILITIES

Appendix C:

Mississippi Center for Advanced Semiconductor Prototyping Facility

The Mississippi Center for Advanced Semiconductor Prototyping (MCASP) is the first university-based SiC prototyping facility established in the world. The center was established in 2000, and is housed initially in a temporary 5,500 square feet facility. Plans are underway to construct a new, permanent facility in the off-campus Mississippi State University Research and Technology Park, which will house 7,500 square feet of class 100 cleanroom and laboratory space. This facility is to be completed in 2002.

LAM 9400 TCP™ etching system designed for 8" Si and modified for SiC in use at MCASP. System has high-density plasma created by 2 RF sources.

MCASP has six full-time technicians, and three full-time engineers (two with Ph.D.'s) for process engineering and materials characterization. MCASP equipment includes a MANN GCA 6300 g-line stepper for alignment to 0.8 μm, donated from Northrop Grumman. A Karl Suss MJB-3 contact aligner provides lower cost lithography for larger features, and a new DUV stepper capable of 0.25 μm alignment is currently being acquired via donation from Phillips. PECVD oxidation equipment (LAM 9900 with Alliance module) and HDP etching equipment (LAM 9400 TCP™ system) are modern, production manufacturing equipment designed for high-throughput 8" Si and modified for SiC. A Hitachi 806 Scanning Electron Microscope (donated from IBM),

automated wafer saw, CVC 601 DC sputter system, Varian 4-pocket e-beam evaporator metal system with ion gun clean, and semi-automatic Wentworth probe stand with MicroManipulator 400°C hot chuck are also included in the MCASP facility. Packaging facilities include a West gold or aluminum wedge bonder. MCASP also has dedicated SUN workstations, with software licenses from both Silvaco and Avant! for two-dimensional device design and simulation.

The equipment, personnel expertise, and management approach define the technical capability of the pilot-production SiC facility at MSU. The principal equipment in MCASP are listed in Table II. All are production grade, multi-wafer systems that are either already available to MSU or are readily commercially available.

MCASP can fabricate SiC transistors and integrated circuits with features as small as 0.8 μm on substrates up to 100-mm (4-in.) in diameter beginning with wafer inspection and continuing (with the exception of out-sourced ion implantation) through wafer-scale testing. Implantation will be out-sourced to a variety of commercial, government or university providers, depending on customer preference and process design. Crucial implant anneals will be performed using silane-based technology developed at MSU. Characterization capabilities include current-voltage (I-V), capacitance-voltage (C-V), deep level transient spectroscopy (DLTS), Admittance Spectroscopy, optical microscopy, and laser-based photoluminescence spectroscopy.

Table II. Overview of major processing and testing equipment in MCASP*.

Equipment	Manufacturer	Source
1. 100-mm multi-wafer SiC epi reactor	Modified production equip.	OEM donation and MCASP modification.
2. G-line 6300 Aligner	GCA	Donation* (Northrop Grumman)
3. High-volume sputter module system	Varian	Donation* (Northrop Grumman)
4. 9400 stand alone plasma etcher	Lam Research	Donation* (Lam Research)
5. 9900 PECVD system w/Alliance II cluster module	Lam Research	Donation* (Lam Research)
6. Oxidation furnace	Thermco or equivalent	Air Force Contract
7. Tri metal E-beam metal evaporator	Varian	Air Force Contract
8. DC sputter system	CVC 601	ONR Contract
9. Microprobe station	Micromanipulator	Air Force Contract
10. IV/CV Characterization system with high-voltage, high-current, low-current resolution	Keithley 237/283 SMU's, Agilent 4156 Semi. Parameter Analyzer, KI 590/595 QS C-V	Air Force Contract

(fA), and high-speed switching matrix.		Donation* (IBM)
11. Hitachi 806C SEM	Hitachi	
12. DUV stepper is a CANON FPA-3000 EX3	Canon	Donation* (Phillips Semiconductor)

*The value of the donated equipment is conservatively estimated at over $2 million.